

Revision History**8Gb(x16) ,16Gb(x32) ,32Gb(x32) LPDDR4x 200ball FBGA PACKAGE**

| Revision | Details | Date |
|----------|---|-----------|
| Rev 1.0 | Initial Release | Apr. 2023 |
| Rev 1.1 | Package Outline Dimension Drawings improved | Aug. 2023 |
| Rev 2.0 | Add 16Gb,32Gb LPDDR4X parts for 2133MHZ | Mar. 2024 |

1 KEY FEATURE

- Double-data rate architecture; two data transfers per clock cycle
- Bidirectional data strobes (DQS_t, DQS_c), These are transmitted/received with data to be used in capturing data at the receiver
- Differential clock inputs (CK_t and CK_c)
- Differential data strobes (DQS_t and DQS_c)
- Commands & addresses entered positive CK edges; data and data mask referenced to both edges of DQS
- 8 internal banks for each channel
- DMI Pin : DBI (Data Bus Inversion) when normal write and read operation, Data mask (DM) for masked write when DBI off
- Counting # of DQ's 1 for masked write when DBI on
- Burst Length: 16, 32 (OTF)
- Burst Type: Sequential
- Read & Write latency : Refer to LPDDR4x AC Timing Table
- Auto Precharge option for each burst access
- Configurable Drive Strength
- Refresh and Self Refresh Modes
- Partial Array Self Refresh and Temperature Compensated Self Refresh
- Write Leveling
- CA Calibration
- Internal VREF and VREF training
- FIFO based write/read training
- MPC (Multi Purpose Command)
- LVSTLE (Low Voltage Swing Terminated Logic Extension) IO
- VDD1/VDD2/VDDQ : 1.8V/1.1V/0.6V
- VSSQ Termination
- No DLL : CK to DQS is not synchronized
- Edge aligned data output, write training for data input center align
- Refresh rate : 3.9us

8Gb = 64M x 16DQ x 8banks x 1channel

16Gb = 64M x 16DQ x 8banks x 2channel

32Gb = 64M x 16DQ x 8banks x 2channels x 2ranks

2 Ordering Information

| Part No. | Density | Org. | Package | Temperature | Max Frequency | Interface |
|-----------------------|---------|-------------|---------------------------|---------------------------|-----------------|-----------|
| AS4C512M16MD4V-053BIN | 8Gb | 1Ch, x16 | 10x15x1.0T(Max), 200-FBGA | Tc = -40 ~ 95°C | 3733Mbps | LVSTLE_06 |
| AS4C512M32MD4V-053BIN | 16Gb | 2ch x32 | 10x15x1.0T(Max), 200-FBGA | Tc = -40 ~ 95°C | 3733Mbps | LVSTLE_06 |
| AS4C512M32MD4V-046BIN | | | 10x15x1.0T(Max), 200-FBGA | Tc = -40 ~ 95°C | 4266Mbps | LVSTLE_06 |
| AS4C1G32MD4V-046BIN | | | 32Gb | 10x15x1.0T(Max), 200-FBGA | Tc = -40 ~ 95°C | 4266Mbps |

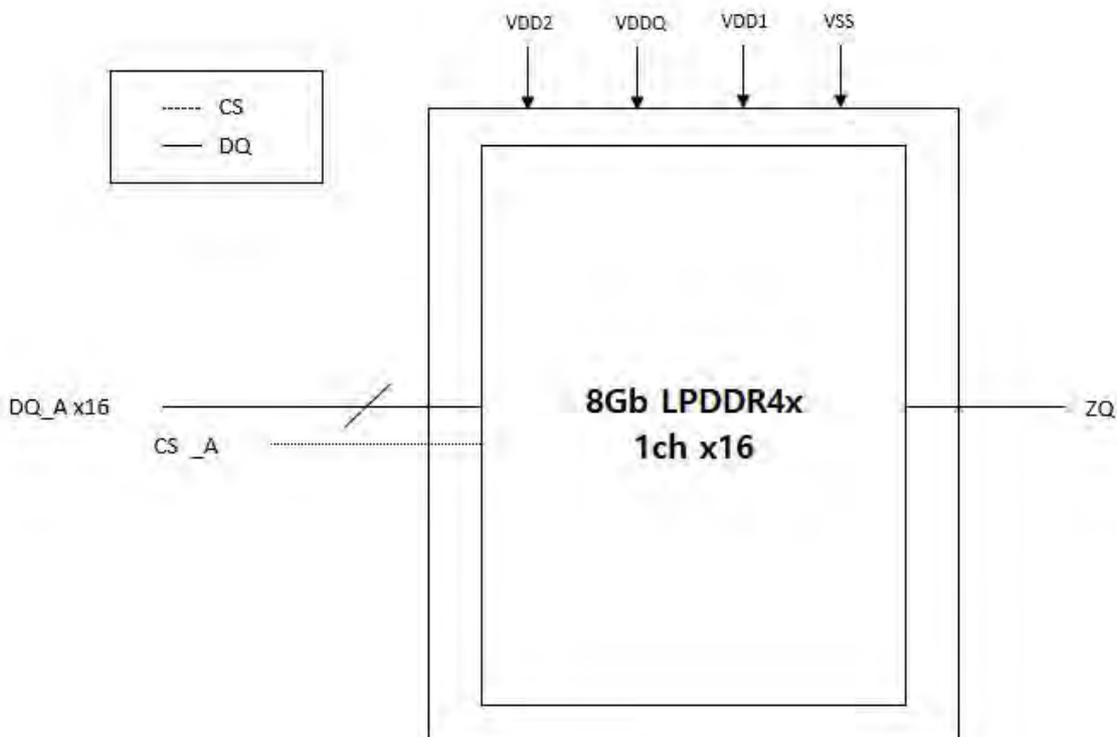
3 PIN DESCRIPTION & Function Diagram

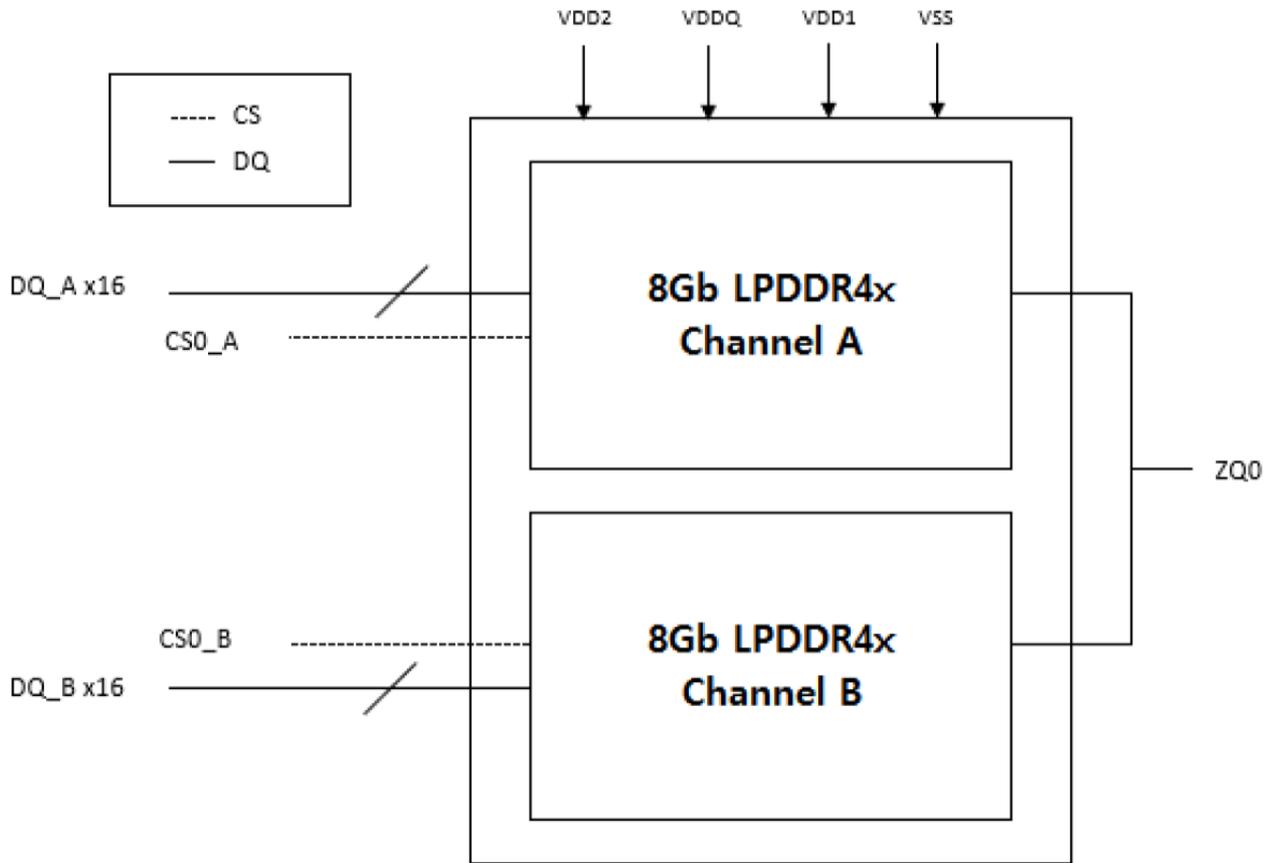
3.0 PIN Description

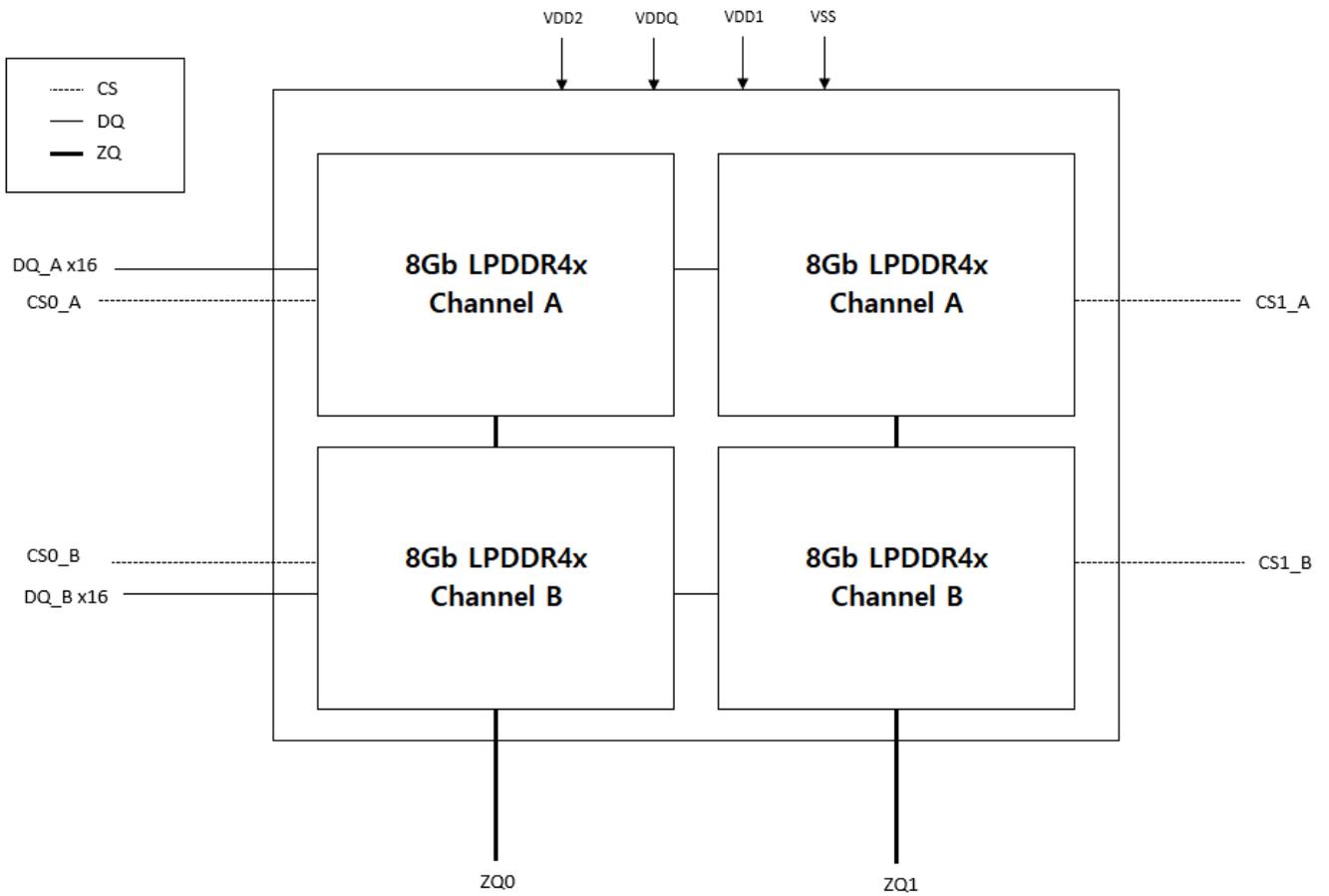
| Pin Name | Pin Function Channel | Pin Name | Pin Function Common |
|---------------|---|------------|---|
| CK_t, CK_c | System Differential Clock | VDD1 | Core Power Supply 1 |
| CKE,CKE0/CKE1 | Clock Enable,CKE for 8Gb and 16Gb, CKE0/CKE1 for 32Gb . | VDD2 | Core Power Supply 2 |
| CS,CS0/CS1 | Chip Select,CS for 8Gb and 16Gb, CS0/CS1 for 32Gb | VDDQ | I/O Power Supply |
| CA[5:0] | DDR Command / Address Inputs | VSS | Ground |
| DMI[1:0] | Input Data Inversion | ZQ,ZQ0/ZQ1 | Reference Pin for Output Driver Strength Calibration. ZQ for 8Gb and 16Gb,ZQ0/ZQ1 for 32Gb. |
| DQS[1:0]_t | Data Strobe Bi-directional | RESET_n | RESET |
| DQS[1:0]_c | Data Strobe Complementary | DNU | Do Not Use |
| DQ[15:0] | Data Inputs / Outputs | | |
| ODT_CA | On die termination | | |

3.1 Functional Block Diagram

8Gb,512M x16 Functional Block Diagram



16Gb,512M x32 Functional Block Diagram


32Gb,1Gx32 Functional Block Diagram


3.2 LPDDR4x Pin Detail Description

[Table 1] Pin Detail Description

Pin Detail Description for 512M x16

| Name | Type | Description |
|------------------------------------|-----------|---|
| CK_t_A, CK_c_A | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. |
| CKE_A, | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. |
| CS_A | Input | Chip Select: CS is part of the command code. |
| CA[5:0]_A | Input | Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. |
| ODT_CA_A | Input | CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. |
| DQ[15:0]_A | I/O | Data Inputs/Outputs: Bi-direction data bus |
| DQS[1:0]_t_A DQS[1:0]_c_A | I/O | Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. |
| DMI[1:0]_A | I/O | Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting. |
| ZQ | Reference | Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor. |
| VDDQ,VDD1, VDD2 | Supply | Power Supplies: Isolated on the die for improved noise immunity. |
| V _{SS} , V _{SSQ} | GND | Ground Reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die. |

Pin Detail Description for 512M x32

| Name | Type | Description |
|--|-----------|---|
| CK_t_A, CK_c_A CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. |
| CKE_A, CKE_B | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. |
| CS_A CS_B | Input | Chip Select: CS is part of the command code. |
| CA[5:0]_A CA[5:0]_B | Input | Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. |
| ODT_CA_A ODT_CA_B | Input | CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. |
| DQ[15:0]_A DQ[15:0]_B | I/O | Data Inputs/Outputs: Bi-direction data bus |
| DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B | I/O | Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. |
| DMI[1:0]_A DMI[1:0]_B | I/O | Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting. |
| ZQ | Reference | Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a $240\Omega \pm 1\%$ resistor. |
| VDDQ,VDD1, VDD2 | Supply | Power Supplies: Isolated on the die for improved noise immunity. |
| V _{SS} , V _{SSQ} | GND | Ground Reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die. |

Pin Detail Description for 1G x32

| Name | Type | Description |
|--|-----------|---|
| CK_t_A, CK_c_A CK_t_B, CK_c_B | Input | Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. |
| CKE0_A, CKE0_B CKE1_A, CKE1_B | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. |
| CS0_A CS0_B CS1_A CS1_B | Input | Chip Select: CS is part of the command code. |
| CA[5:0]_A CA[5:0]_B | Input | Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. |
| ODT_CA_A ODT_CA_B | Input | CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. |
| DQ[15:0]_A DQ[15:0]_B | I/O | Data Inputs/Outputs: Bi-direction data bus |
| DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B | I/O | Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. |
| DMI[1:0]_A DMI[1:0]_B | I/O | Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting. |
| ZQ0, ZQ1 | Reference | Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to VDDQ through a 240Ω ± 1% resistor. |
| VDDQ,VDD1, VDD2 | Supply | Power Supplies: Isolated on the die for improved noise immunity. |
| Vss, Vssq | GND | Ground Reference: Power supply ground reference. |
| RESET_n | Input | RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die. |

3.3 LPDDR4x SDRAM Package Ballout

200-ball 512M x16 Discrete Package, 0.80mm x 0.65mm

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------------------|----------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|----|
| A | NC | NC | VSS | V _{DD2} | ZQ | 0.80mm Pitch | | NC | V _{DD2} | VSS | DNU | NC |
| B | NC | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | NC | |
| C | VSS | DQ1_A | DMI0_A | DQ6_A | VSS | | VSS | DQ14_A | DMI1_A | DQ9_A | VSS | |
| D | V _{DDQ} | VSS | DQS0_T_A | VSS | V _{DDQ} | | V _{DDQ} | VSS | DQS1_T_A | VSS | V _{DDQ} | |
| E | VSS | DQ2_A | DQS0_C_A | DQ5_A | VSS | | VSS | DQ13_A | DQS1_C_A | DQ10_A | VSS | |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} | |
| G | VSS | ODT_CA_A | VSS | V _{DD1} | VSS | | VSS | V _{DD1} | VSS | NC | VSS | |
| H | V _{DD2} | CA0_A | NC | CS_A | V _{DD2} | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} | |
| J | VSS | CA1_A | VSS | CKE_A | NC | | CK_t_A | CK_c_A | VSS | CA5_A | VSS | |
| K | V _{DD2} | VSS | V _{DD2} | VSS | NC | | NC | VSS | V _{DD2} | VSS | V _{DD2} | |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | V _{DD2} | VSS | V _{DD2} | VSS | NC | | NC | VSS | V _{DD2} | VSS | V _{DD2} | |
| P | VSS | NC | VSS | NC | NC | | NC | NC | VSS | NC | VSS | |
| R | V _{DD2} | NC | NC | NC | V _{DD2} | | V _{DD2} | NC | NC | NC | V _{DD2} | |
| T | VSS | NC | VSS | V _{DD1} | VSS | | VSS | V _{DD1} | VSS | RESET_n | VSS | |
| U | V _{DD1} | NC | V _{DDQ} | NC | V _{DD2} | V _{DD2} | NC | V _{DDQ} | NC | V _{DD1} | | |
| V | VSS | NC | NC | NC | VSS | VSS | NC | NC | NC | VSS | | |
| W | V _{DDQ} | VSS | NC | VSS | V _{DDQ} | V _{DDQ} | VSS | NC | VSS | V _{DDQ} | | |
| Y | VSS | NC | NC | NC | VSS | VSS | NC | NC | NC | VSS | | |
| AA | NC | NC | V _{DDQ} | NC | V _{DDQ} | V _{DDQ} | NC | V _{DDQ} | NC | NC | | |
| AB | NC | NC | VSS | V _{DD2} | VSS | VSS | V _{DD2} | VSS | NC | NC | | |

[Top View]

NOTE :

- 1) ODT(CA)_[x] balls are wired to ODT(CA)_[x] pads of Rank 0 DRAM die. ODT(CA)_[x] pads for other ranks (if present) are disabled in the package.
- 2) In case ODT function is not used, ODT pin should be considered as NC.
- 3) ODT will be connected to rank 0. The ODT Input to rank 1 (if 2nd rank is present) will be connected to ground in the package
- 4) 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows and Top view, A1 in top left corner

200-ball 512M x32 Discrete Package, 0.80mm x 0.65mm

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|----|------------------|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|--------|------------------|
| A | NC | NC | VSS | V _{DD2} | ZQ | 0.80mm Pitch | | NC | V _{DD2} | VSS | NC | NC |
| B | NC | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | NC |
| C | VSS | DQ1_A | DMI0_A | DQ6_A | VSS | | | VSS | DQ14_A | DMI1_A | DQ9_A | VSS |
| D | V _{DDQ} | VSS | DQS0_T_A | VSS | V _{DDQ} | | | V _{DDQ} | VSS | DQS1_T_A | VSS | V _{DDQ} |
| E | VSS | DQ2_A | DQS0_C_A | DQ5_A | VSS | | | VSS | DQ13_A | DQS1_C_A | DQ10_A | VSS |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} |
| G | VSS | ODT_CA_A*1 | VSS | V _{DD1} | VSS | | | VSS | V _{DD1} | VSS | NC | VSS |
| H | V _{DD2} | CA0_A | NC | CS_A | V _{DD2} | | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} |
| J | VSS | CA1_A | VSS | CKE_A | NC | | | CK_t_A | CK_c_A | VSS | CA5_A | VSS |
| K | V _{DD2} | VSS | V _{DD2} | VSS | NC | | | NC | VSS | V _{DD2} | VSS | V _{DD2} |
| L | | | | | | | | | | | | |
| M | | | | | | | | | | | | |
| N | V _{DD2} | VSS | V _{DD2} | VSS | NC | | | NC | VSS | V _{DD2} | VSS | V _{DD2} |
| P | VSS | CA1_B | VSS | CKE_B | NC | CK_t_B | CK_c_B | VSS | CA5_B | VSS | | |
| R | V _{DD2} | CA0_B | NC | CS_B | V _{DD2} | V _{DD2} | CA2_B | CA3_B | CA4_B | V _{DD2} | | |
| T | VSS | ODT_CA_B*1 | VSS | V _{DD1} | VSS | VSS | V _{DD1} | VSS | RESET_n | VSS | | |
| U | V _{DD1} | DQ3_B | V _{DDQ} | DQ4_B | V _{DD2} | V _{DD2} | DQ12_B | V _{DDQ} | DQ11_B | V _{DD1} | | |
| V | VSS | DQ2_B | DQS0_C_B | DQ5_B | VSS | VSS | DQ13_B | DQS1_C_B | DQ10_B | VSS | | |
| W | V _{DDQ} | VSS | DQS0_T_B | VSS | V _{DDQ} | V _{DDQ} | VSS | DQS1_T_B | VSS | V _{DDQ} | | |
| Y | VSS | DQ1_B | DMI0_B | DQ6_B | VSS | VSS | DQ14_B | DMI1_B | DQ9_B | VSS | | |
| AA | NC | DQ0_B | V _{DDQ} | DQ7_B | V _{DDQ} | V _{DDQ} | DQ15_B | V _{DDQ} | DQ8_B | NC | | |
| AB | NC | NC | VSS | V _{DD2} | VSS | VSS | V _{DD2} | VSS | NC | NC | | |

NOTE :

[Top View]

- 1) ODT(CA)_[x] balls are wired to ODT(CA)_[x] pads of Rank 0 DRAM die. ODT(CA)_[x] pads for other ranks (if present) are disabled in the package.
- 2) In case ODT function is not used, ODT pin should be considered as NC.
- 3) ODT will be connected to rank 0. The ODT Input to rank 1 (if 2nd rank is present) will be connected to ground in the package

200-ball 1Gx32 Discrete Package, 0.80mm x 0.65mm

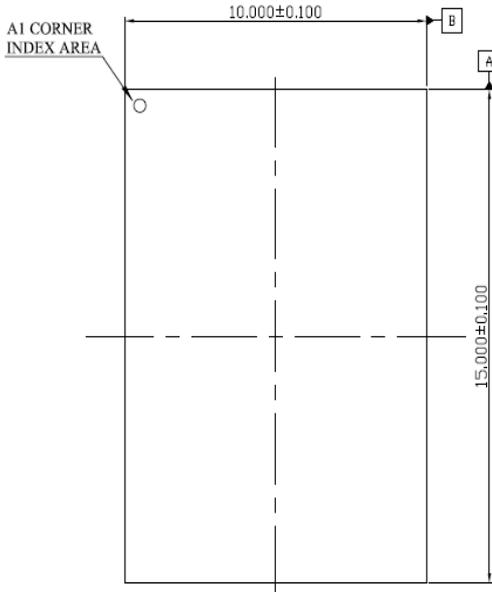
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | |
|----|------------------|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A | NC | NC | VSS | V _{DD2} | ZQ0 | 0.80mm Pitch | | ZQ1 | V _{DD2} | VSS | NC | NC | |
| B | NC | DQ0_A | V _{DDQ} | DQ7_A | V _{DDQ} | | | V _{DDQ} | DQ15_A | V _{DDQ} | DQ8_A | NC | NC |
| C | VSS | DQ1_A | DMI0_A | DQ6_A | VSS | | | VSS | DQ14_A | DMI1_A | DQ9_A | VSS | VSS |
| D | V _{DDQ} | VSS | DQS0_T_A | VSS | V _{DDQ} | | | V _{DDQ} | VSS | DQS1_T_A | VSS | VSS | V _{DDQ} |
| E | VSS | DQ2_A | DQS0_C_A | DQ5_A | VSS | | | VSS | DQ13_A | DQS1_C_A | DQ10_A | VSS | VSS |
| F | V _{DD1} | DQ3_A | V _{DDQ} | DQ4_A | V _{DD2} | | | V _{DD2} | DQ12_A | V _{DDQ} | DQ11_A | V _{DD1} | V _{DD1} |
| G | VSS | ODT_CA_A*1 | VSS | V _{DD1} | VSS | | | VSS | V _{DD1} | VSS | NC | VSS | VSS |
| H | V _{DD2} | CA0_A | CS1_A | CS0_A | V _{DD2} | | | V _{DD2} | CA2_A | CA3_A | CA4_A | V _{DD2} | V _{DD2} |
| J | VSS | CA1_A | VSS | CKE0_A | CKE1_A | | | CK_t_A | CK_c_A | VSS | CA5_A | VSS | VSS |
| K | V _{DD2} | VSS | V _{DD2} | VSS | NC | | | NC | VSS | V _{DD2} | VSS | VSS | V _{DD2} |
| L | | | | | | | | | | | | | |
| M | | | | | | | | | | | | | |
| N | V _{DD2} | VSS | V _{DD2} | VSS | NC | | | NC | VSS | V _{DD2} | VSS | V _{DD2} | V _{DD2} |
| P | VSS | CA1_B | VSS | CKE0_B | CKE1_B | | | CK_t_B | CK_c_B | VSS | CA5_B | VSS | VSS |
| R | V _{DD2} | CA0_B | CS1_B | CS0_B | V _{DD2} | V _{DD2} | CA2_B | CA3_B | CA4_B | V _{DD2} | V _{DD2} | | |
| T | VSS | ODT_CA_B*1 | VSS | V _{DD1} | VSS | VSS | V _{DD1} | VSS | RESET_n | VSS | VSS | | |
| U | V _{DD1} | DQ3_B | V _{DDQ} | DQ4_B | V _{DD2} | V _{DD2} | DQ12_B | V _{DDQ} | DQ11_B | V _{DD1} | V _{DD1} | | |
| V | VSS | DQ2_B | DQS0_C_B | DQ5_B | VSS | VSS | DQ13_B | DQS1_C_B | DQ10_B | VSS | VSS | | |
| W | V _{DDQ} | VSS | DQS0_T_B | VSS | V _{DDQ} | V _{DDQ} | VSS | DQS1_T_B | VSS | VSS | V _{DDQ} | | |
| Y | VSS | DQ1_B | DMI0_B | DQ6_B | VSS | VSS | DQ14_B | DMI1_B | DQ9_B | VSS | VSS | | |
| AA | NC | DQ0_B | V _{DDQ} | DQ7_B | V _{DDQ} | V _{DDQ} | DQ15_B | V _{DDQ} | DQ8_B | NC | NC | | |
| AB | NC | NC | VSS | V _{DD2} | VSS | VSS | V _{DD2} | VSS | NC | NC | NC | | |

NOTE :

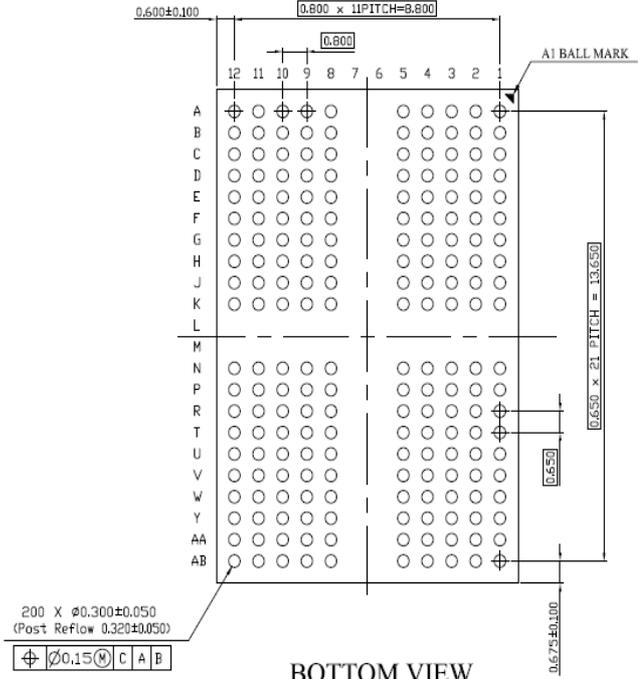
[Top View]

- 1) ODT(CA)_[x] balls are wired to ODT(CA)_[x] pads of Rank 0 DRAM die. ODT(CA)_[x] pads for other ranks (if present) are disabled in the package.
- 2) In case ODT function is not used, ODT pin should be considered as NC.
- 3) ODT will be connected to rank 0. The ODT Input to rank 1 (if 2nd rank is present) will be connected to ground in the package

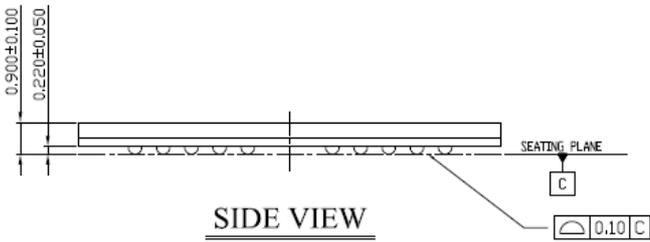
3.4 LPDDR4x SDRAM Package Dimension



TOP VIEW



BOTTOM VIEW



SIDE VIEW

NOTE :

1. ALL DIMENSION ARE IN MILLIMETERS.

4 FUNCTIONAL DESCRIPTION

The Low Power DDR4X (LPDDR4X) SDRAM is a high-speed synchronous Dynamic random-access memory internally configured with either 1 or 2 channels. Each channel is comprised of 16DQs and 8-banks. Refer to Table.2 for details of architecture.

This device contains the following number of bits:

8Gb has 8,589,934,592 bits,16Gb has 17,179,869,184 bits and 32Gb has 34,359,738,368 bits .

LPDDR4X devices use a 2 or 4 clocks architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 6-bit CA bus contains command, address, and bank information. Each command uses 1, 2 or 4 clock cycle, during which command information is transferred on the positive edge of the clock. See command truth table for details.

These devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially an 16n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR4X SDRAM effectively consists of a single 16n-bit wide, one clock cycle data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins. Read and write accesses to the LPDDR4X SDRAMs are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an Activate command, which is then followed by a Read, Write or Mask Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read, Write or Mask Write command are used to select the Bank and the starting column location for the burst access.

Prior to normal operation, the LPDDR4X SDRAM must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

4.1 LPDDR4x ADDRESSING

[Table 2] LPDDR4x Addressing

| Memory Density | | 8Gb | 16Gb | 32Gb |
|--------------------------------------|------------------------------------|------------------------------------|------------------------------------|--|
| Memory Density (per Die) | | 8Gb | 8Gb, Dual Dies | 8Gb, Quad Dies |
| Configuration | | 64Mb x 16DQ x 8 banks x 1 channels | 64Mb x 16DQ x 8 banks x 2 channels | 64Mb x 16DQ x 8 banks x 2 channels x 2cs |
| Number of Channels | | 1 | 2 | 2 |
| Number of Banks (per channel) | | 8 | 8 | 8 |
| Array Pre-Fetch (bits, per channel) | | 256 | 256 | 256 |
| Number of Rows (per Channel) | | 65,536 | 65,536 | 65,536 |
| Number of Columns (fetch boundaries) | | 64 | 64 | 64 |
| Page Size (Bytes) | | 2048 | 2048 | 2048 |
| Channel Density | | 8,589,934,592 | 8,589,934,592 | 17,179,869,184 |
| Total Density | | 8,589,934,592 | 17,179,869,184 | 34,359,738,368 |
| Bank Addresses | | BA0-BA2 | BA0-BA2 | BA0-BA2 |
| x16 | Row Addresses ²⁾ | R0-R15 | R0-R15 | R0-R15 |
| | Column Addresses ^{1), 2)} | C0-C9 | C0-C9 | C0-C9 |
| Burst Starting Address Boundary | | 64 - bit | 64 - bit | 64 - bit |

NOTE :

1) The lower two column addresses (C0-C1) are assumed to be "zero" and are not transmitted on the CA bus.

2) Row and ColumnAddress values on the CA bus that are not used for a particular density be at valid logic levels.

3) For non - binary memory densities, only quarter of the row address space is invalid. When the MSB address bit is "HIGH", then the MSB - 1 address bit must be "LOW".

4) The row address input which violates restriction described in note 3 in this table may result in undefined or vendor specific behavior. Consult memory vendor for more information.

4.2 Simplified LPDDR4x State Diagram

LPDDR4x state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification. The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

For the command definition, see datasheet of [Command Definition & Timing Diagram].

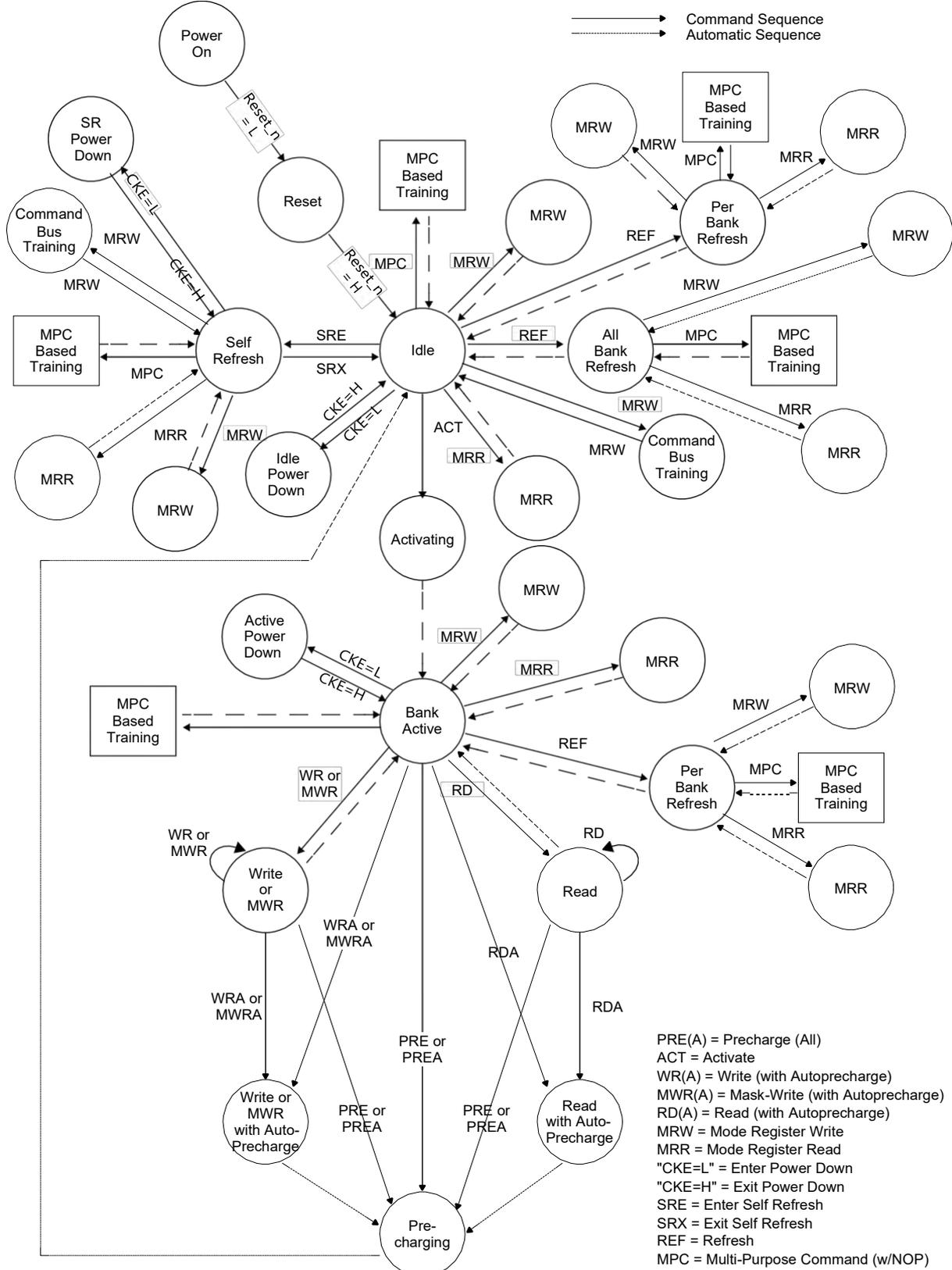


Figure 1. LPDDR4x: Simplified Bus Interface State Diagram-1

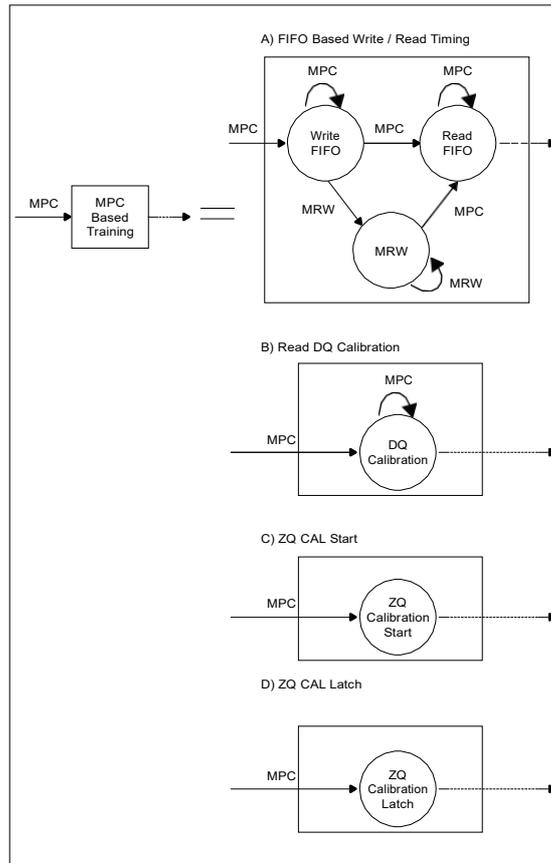


Figure 2. LPDDR4x: Simplified Bus Interface State Diagram -2

NOTE :

- 1) From the Self-Refresh state the device can enter Power-Down, MRR, MRW, or MPC states. See the section on Self-Refresh for more information.
- 2) In IDLE state, all banks are precharged.
- 3) In the case of a MRW command to enter a training mode, the state machine will not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
- 4) In the case of a MPC command to enter a training mode, the state machine may not automatically return to the IDLE state at the conclusion of training. See the applicable training section for more information.
- 5) This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than one bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.
- 6) States that have an "automatic return" and can be accessed from more than one prior state (Ex. MRW from either Idle or Active states) will return to the state from when they were initiated (Ex. MRW from Idle will return to Idle).
- 7) The RESET_n pin can be asserted from any state, and will cause the SDRAM to go to the Reset State. The diagram shows RESET applied from the Power-On as an example, but the Diagram should not be construed as a restriction on RESET_n.

4.2.1 Power-up and Initialization

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as following table.

[Table 3] MRS defaults settings

| Item | MRS | Default setting | Description |
|------------------|--------------|-----------------|---------------------------------|
| FSP-OP/WR | MR13 OP[7:6] | 00B | FS-OP/WR[0] are enabled |
| WLS | MR2 OP[6] | 0B | Write Latency Set 0 is selected |
| WL | MR2 OP[5:3] | 000B | WL = 4 |
| RL | MR2 OP[2:0] | 000B | RL = 6, nRTP = 8 |
| nWR | MR1 OP[6:4] | 000B | nWR = 6 |
| DBI-WR/RD | MR3 OP[7:6] | 00B | Write & Read DBI are disabled |
| CA ODT | MR11 OP[6:4] | 000B | CA ODT is disabled |
| DQ ODT | MR11 OP[2:0] | 000B | DQ ODT is disabled |
| Vref(ca) Setting | MR12 OP[6] | 1B | Vref(ca) Range[1] enabled |
| Vref(ca) value | MR12 OP[5:0] | 011101B | Range1: 50.4% of VDDQ |
| Vref(DQ) Setting | MR14 OP[6] | 1B | Vref(DQ) Range[1] enabled |
| Vref(DQ) Value | MR14 OP[5:0] | 011101B | Range1: 50.4% of VDDQ |

4.2.1.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW ($\leq 0.2 \times VDD2$) and all inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_n is held LOW. Power supply voltage ramp requirements are provided in Table - Voltage Ramp Conditions. VDD1 must ramp at the same time or earlier than VDD2. VDD2 must ramp at the same time or earlier than VDDQ.

[Table 4] Voltage Ramp Conditions

| After... | Applicable Conditions |
|---------------|--|
| Ta is reached | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

NOTE :

- 1) Ta is the point when any power supply first reaches 300mV.
 - 2) Voltage ramp conditions in above table apply between Ta and power-off (controlled or uncontrolled).
 - 3) Tb is the point at which all supply and reference voltages are within their defined ranges.
 - 4) Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
 - 5) The voltage difference between any of VSS and VSSQ pins must not exceed 100mV.
2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between Vssq and Vddq during voltage ramp to avoid latch-up. CKE, CK_t, CK_c, CS_n and CA input levels must be between Vss and VDD2 during voltage ramp to avoid latch-up.
 3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be de-asserted to HIGH(Tc). At least 10ns before CKE de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

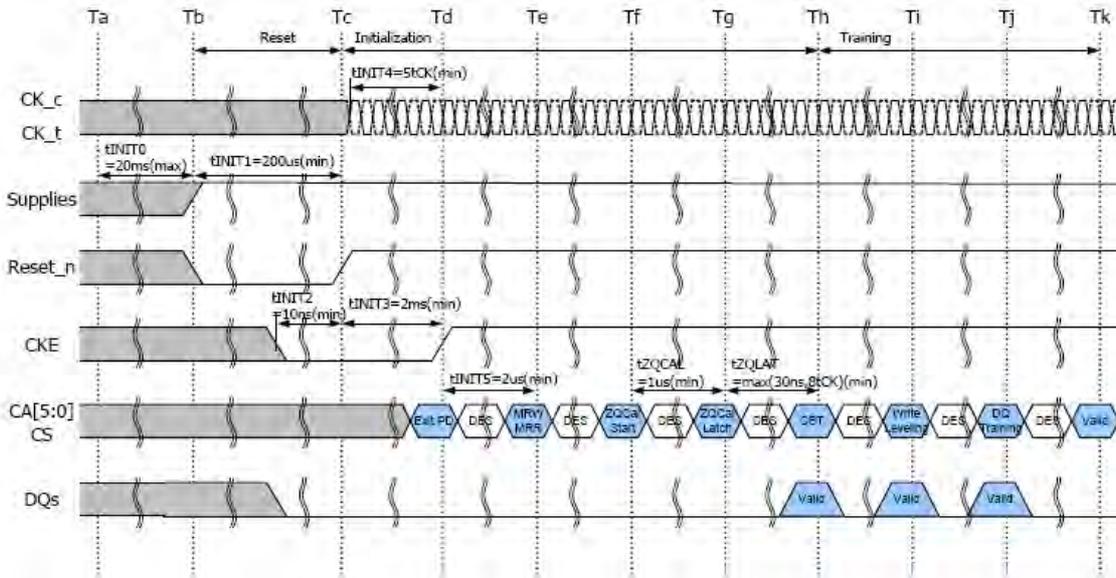


Figure 3. Power Ramp and Initialization Sequence

NOTE :

- 1) Training is optional and may be done at the system architect's discretion. The training sequence after ZQ_CAL Latch (Th, Sequence 7~9) in the above figure, is a simplified recommendation and actual training sequence may vary depending on systems.
4. After RESET_n is de-asserted (Tc), wait at least tINIT3 before activating CKE. Clock (CK_t, CK_c) is required to be started and stabilized for tINIT4 before CKE goes active (Td). CS is required to be maintained LOW when controller activates CKE.
5. After setting CKE high, wait a minimum of tINIT5 to issue any MRR or MRW commands (Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSK) could have relaxed timings (such as tDQSKb) before the system is appropriately configured.
6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory (Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.
7. After tZQLAT is satisfied (Th) the command bus (internal VREF(ca), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal VREF and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and VREF(ca) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.
The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See command bus training in the MRW section for information on how to enter/ exit the training mode.
8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See write leveling section for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal VREF(dq), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust VREF(dq)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and VREF(dq) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.
10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

[Table 5] Initialization Timing Parameters

| Parameter | Value | | Unit | Comment |
|-----------|----------------|-----------|------|---|
| | Min | Max | | |
| tINIT0 | | 20 | ms | Maximum Voltage Ramp Time |
| tINIT1 | 200 | | us | Minimum RESET_n LOW time after completion of voltage ramp |
| tINIT2 | 10 | | ns | Minimum CKE LOW time before RESET_n goes HIGH |
| tINIT3 | 2 | | ms | Minimum CKE LOW time after RESET_n goes HIGH |
| tINIT4 | 5 | | tCK | Minimum stable clock before first CKE HIGH |
| tINIT5 | 2 | | us | Minimum idle time before first MRW/MRR command |
| tZQCAL | 1 | | us | ZQ Calibration time |
| tZQLAT | Max(30ns,8tCK) | | ns | ZQCAL latch quite time |
| tCKb | Note 1, 2 | Note 1, 2 | ns | Clock cycle time during boot |

NOTE :

- 1) Min tCKb guaranteed by DRAM test is 18ns.
- 2) The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent

4.2.1.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x VDD2 anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n
2. Repeat steps 4 to 10 in "Voltage Ramp and Device Initialization" section.

[Table 6] Reset Timing Parameters

| Parameter | Value | | Unit | Comment |
|-----------|-------|-----|------|---|
| | Min | Max | | |
| tPW_RESET | 100 | - | ns | Minimum RESET_n low time for Reset Initialization with stable power |

4.2.2 Power-off Sequence

4.2.2.1 Controlled Power-off

The following procedure is required to power off the device.

While powering off, CKE must be held LOW ($\leq 0.2 \times VDD2$) and all other inputs must be between V_{ILmin} and V_{IHmax} .

The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and $VDDQ$ during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and $VDD2$ during voltage ramp to avoid latch-up.

T_x is the point where any power supply drops below the minimum value specified.

T_z is the point where all power supplies are below 300mV. After T_z, the device is powered off.

[Table 7] Power Supply Conditions for Power-off

| Between... | Applicable Conditions |
|------------|--|
| TX and TZ | VDD1 must be greater than VDD2 |
| | VDD2 must be greater than VDDQ - 200mV |

NOTE :

- 1) The voltage difference between any of V_{SS} , V_{SSQ} pins must not exceed 100mV

4.2.2.2 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At T_x, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After T_z (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative voltage between power supplies is uncontrolled. $VDD1$ and $VDD2$ must decrease with a slope lower than $0.5V/\mu s$ between T_x and T_z.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

[Table 8] Timing Parameters for Power-off

| Symbol | Value | | Unit | Comment |
|--------|-------|-----|------|-----------------------------|
| | Min | Max | | |
| tPOFF | | 2 | s | Maximum Power-off ramp time |

4.3 Mode Register Definition

4.3.1 Mode Register Assignment and Definition in LPDDR4x

shows the mode registers for LPDDR4x. Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

[Table 9] Mode Register Assignment in LPDDR4x

| MR# | MA <7:0> | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | |
|-----|-----------------|---|--------|---|----------------|-------------------|----------|----------------|--------|---------|--------------|----------|
| 0 | 00 _H | Device Info. | R | CATR | RFU | Single Ended mode | RZQI | | (RFU) | | Refresh mode | |
| 1 | 01 _H | Device Feature 1 | W | RPST0 | nWR0 | | RD-PRE0 | WR-PRE0 | BL | | | |
| | | | | RPST1 | nWR1 | | RD-PRE1 | WR-PRE1 | | | | |
| 2 | 02 _H | Device Feature 2 | W | WR Lev | WL Select0 | WL0 | | RL0 | | | | |
| | | | | | WL Select1 | WL1 | | RL1 | | | | |
| 3 | 03 _H | I/O Configuration-1 | W | DBI-WR0 | DBI-RD0 | PDDS0 | | PPR Protection | WR PST | PU-CAL0 | | |
| | | | | DBI-WR1 | DBI-RD1 | PDDS1 | | | WR PST | PU-CAL1 | | |
| 4 | 04 _H | Refresh Rate | R/W | TUF | Thermal Offset | PPRE | SR Abort | Refresh Rate | | | | |
| 5 | 05 _H | Basic Configuration-1 | R | LPDDR4x Manufacturer ID | | | | | | | | |
| 6 | 06 _H | Basic Configuration-2 | R | Revision ID-1 | | | | | | | | |
| 7 | 07 _H | Basic Configuration-3 | R | Revision ID-2 | | | | | | | | |
| 8 | 08 _H | Basic Configuration-4 | R | I/O width | Density | | | | Type | | | |
| 9 | 09 _H | Test Mode | W | Vendor Specific Test Register | | | | | | | | |
| 10 | 0A _H | IO Calibration | W | (RFU) | | | | | | | | ZQ-RESET |
| 11 | 0B _H | ODT Feature | W | (RFU) | CA ODT0 | | (RFU) | DQ ODT0 | | | | |
| | | | | | CA ODT1 | | | DQ ODT1 | | | | |
| 12 | 0C _H | VREF(ca) Setting/Range | R/W | (RFU) | VR-CA0 | VREF0(ca) | | | | | | |
| | | | | (RFU) | VR-CA1 | VREF1(ca) | | | | | | |
| 13 | 0D _H | CBT,RPT,VRO,VRCG, RRO, DM_DIS,FSP-WR,FSP-OP | W | FSP-OP | FSP-WR | DM_DIS | RRO | VRCG | VRO | RPT | CBT | |
| 14 | 0E _H | VREF(dq) Setting/Range | R/W | (RFU) | VR-DQ0 | VREF0(DQ) | | | | | | |
| | | | | (RFU) | VR-DQ1 | VREF1(DQ) | | | | | | |
| 15 | 0F _H | Lower-Byte Invert for DQ Calibration | W | Lower-Byte Invert Register for DQ Calibration | | | | | | | | |
| 16 | 10 _H | PASR_Bank | W | PASR Bank Mask | | | | | | | | |
| 17 | 11 _H | PASR_Segment | W | PASR Segment Mask | | | | | | | | |
| 18 | 12 _H | IT-LSB | R | DQS Oscillator Count-LSB | | | | | | | | |
| 19 | 13 _H | IT-MSB | R | DQS Oscillator Count-MSB | | | | | | | | |
| 20 | 14 _H | Upper-Byte Invert for DQ Calibration | W | Upper-Byte Invert Register for DQ Calibration | | | | | | | | |
| 21 | 15 _H | RFU | N/A | (RFU) | | | | | | | | |
| 22 | 16 _H | ODT Feature | W | (RFU) | ODT-CA0 | ODT-CS0 | ODT-CK0 | SoC ODT0 | | | | |
| | | | | (RFU) | ODT-CA1 | ODT-CS1 | ODT-CK1 | SoC ODT1 | | | | |

[Table 9] Mode Register Assignment in LPDDR4x (Continued)

| MR# | MA <7:0> | Function | Access | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----------------------------------|-----------------------------|--------|--|--------------|--------|--------|--------------------|-------------------|-------------------|--------|
| 23 | 17 _H | DQS interval timer runtime | W | DQS interval timer run time setting | | | | | | | |
| 24 | 18 _H | TRR | R/W | TRR Mode | TRR Mode BAn | | | Unlim-ited MAC | MAC Value | | |
| 25 | 19 _H | PPR Resource | R | Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |
| 26:29 | 1A _H : 1D _H | RFU | N/A | Reserved for Future Use | | | | | | | |
| 30 | 1E _H | Reserved for Testing | N/A | Reserved for Testing-SDRAM will ignore | | | | | | | |
| 31 | 1F _H | RFU | N/A | Reserved for Future Use | | | | | | | |
| 32 | 20 _H | DQ Calibration Pattern A | W | DQ Calibration Pattern "A" (default = 5AH) | | | | | | | |
| 33:38 | 21 _H ~26 _H | (Do Not Use) | NA | Do Not Use | | | | | | | |
| 39 | 27 _H | Reserved for Testing | N/A | Reserved for Testing-SDRAM will ignore | | | | | | | |
| 40 | 28 _H | DQ Calibration Pattern B | W | DQ Calibration Pattern "B" (default = 3CH) | | | | | | | |
| 41:47 | 29 _H ~2F _H | (Do Not Use) | NA | Do Not Use | | | | | | | |
| 48:50 | 30 _H ~32 _H | RFU | NA | (RFU) | | | | | | | |
| 51 | 33 _H | Single Ended RDQS, WDQS,CLK | W | (RFU) | | | | Single Ended Clock | Single Ended WDQS | Single Ended RDQS | (RFU) |
| 52:63 | 34 _H ~3F _H | RFU | NA | (RFU) | | | | | | | |

| | |
|--|----------------------|
| | Applied when FSP = 0 |
| | Applied when FSP = 1 |

NOTE :

- 2) RFU bits shall be set to '0' during writes.
- 3) RFU bits shall be read as '0' during reads.
- 4) All mode registers that are specified as RFU or write-only shall return undefined data when read and DQS_t, DQS_c shall be toggled.
- 5) All mode registers that are specified as RFU shall not be written.
- 6) Writes to read-only registers shall have no impact on the functionality of the device.

MR0_Device Information (MA<7:0> = 00_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|------|-------|-------------------|------|-----|-------|-----|--------------|
| CATR | (RFU) | Single ended mode | RZQI | | (RFU) | | Refresh mode |

| Function | Register Type | Operand | Data | Notes |
|--------------------------------------|---------------|---------|---|---------|
| Refresh mode | Read-only | OP[0] | 0_B : Both legacy & modified refresh mode supported 1_B : Only modified refresh mode supported | |
| RZQI (Built-in Self-Test for RZQ) | | OP[4:3] | 00_B : RZQ self-test not supported 01_B : ZQ-pin may connect to V _{SSQ} or float 10_B : ZQ-pin may short to V _{DDQ} 11_B : ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to V _{SSQ} or float, nor short to V _{DDQ}) | 1,2,3,4 |
| Single ended mode | | OP[5] | 0_B : No support for Single ended mode 1_B : Supports for Single ended mode | 6 |
| CATR (CA Terminating Rank) | | OP[7] | 0_B : CA for this rank is not terminated 1_B : Vendor specific | 5 |

NOTE :

1) RZQI MR value, if supported, will be valid after the following sequence:

- a. Completion of MPC ZQCAL Start command to either channel.
- b. Completion of MPC ZQCAL Latch command to either channel then t_{ZQLAT} is satisfied.

RZQI value will be lost after Reset.

2) If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01_B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01_B or OP[4:3] = 10_B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.

3) In the case of possible assembly error, the LPDDR4x device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the device may not function as intended.

4) In ZQ self-test returns OP[4:3] = 11_B, the device has detected a resistor connected to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e 240-Ω +/- 1%).

5) CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.

6) Support for Single Ended Mode is optional. If supported, Single Ended Write DQS, Read DQS and CK can be enabled in MR51

MR1_Device Feature 1 (MA<7:0> = 01_H) :

| | | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 | |
|---|---------------|---------|--------------|-----|---|--------|--------|-----|-------|--|
| | | RPST | nWR (for AP) | | | RD-PRE | WR-PRE | BL | | |
| Function | Register Type | Operand | | | Data | | | | Notes | |
| BL (Burst Length) | Write-only | OP[1:0] | | | 00_B : BL=16 Sequential (default) 01_B : BL=32 Sequential 10_B : BL=16 or 32 Sequential (on-the-fly) All others : Reserved | | | | 1 | |
| WR-PRE (WR Pre-amble Length) | | OP[2] | | | 0_B : Reserved 1_B : WR Pre-amble = 2×tCK | | | | 5,6 | |
| RD-PRE (RD Pre-amble Type) | | OP[3] | | | 0_B : RD Pre-amble = Static (default) 1_B : RD Pre-amble = Toggle | | | | 3,5,6 | |
| nWR (Write-Recovery for Auto-Precharge commands) | | OP[6:4] | | | 000_B : nWR = 6 (default) 001_B : nWR = 10 010_B : nWR = 16 011_B : nWR = 20 100_B : nWR = 24 101_B : nWR = 30 110_B : nWR = 34 111_B : nWR = 40 | | | | 2,5,6 | |
| RPST (RD Post-Ambles Length) | | OP[7] | | | 0_B : RD Post-ambles = 0.5×tCK (default) 1_B : RD Post-ambles = 1.5×tCK | | | | 4,5,6 | |

- NOTE :**
- Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.
 - The programmed value of nWR is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled. See , "Frequency Ranges for RL, WL, and nWR Settings" later in this section.
 - For Read operations this bit must be set to select between a “toggling” pre-ambles and a “Non-toggling” pre-ambles. See the Read Preamble and Postambles section in Operation timing for a drawing of each type of pre-ambles.
 - OP[7] provides an optional READ post-ambles with an additional rising and falling edge of DQS_t. The optional postambles cycle is provided for the benefit of certain memory controllers.
 - There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
 - Supporting the two physical registers for Burst Length: MR1 OP[1:0] as optional feature. Applications requiring support of both vendor options shall assure that both FSP-OP[0] and FSP-OP[1] are set to the same code. Refer to vendor datasheets for detail.

[Table 10] Read and Write Latencies

| Read Latency | | Write Latency | | nWR | nRTP | Lower Clock Frequency Limit (Greater than) | Upper Clock Frequency Limit (Same or less than) | Units | Notes |
|--------------|--------|---------------|---------|-----|------|--|---|-------|-------------|
| No DBI | w/ DBI | Set "A" | Set "B" | | | | | | |
| 6 | 6 | 4 | 4 | 6 | 8 | 10 | 266 | MHz | 1,2,3,4,5,6 |
| 10 | 12 | 6 | 8 | 10 | 8 | 266 | 533 | | |
| 14 | 16 | 8 | 12 | 16 | 8 | 533 | 800 | | |
| 20 | 22 | 10 | 18 | 20 | 8 | 800 | 1066 | | |
| 24 | 28 | 12 | 22 | 24 | 10 | 1066 | 1333 | | |
| 28 | 32 | 14 | 26 | 30 | 12 | 1333 | 1600 | | |
| 32 | 36 | 16 | 30 | 34 | 14 | 1600 | 1866 | | |
| 36 | 40 | 18 | 34 | 40 | 16 | 1866 | 2133 | | |

- NOTE :**
- The LPDDR4x device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
 - DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0_B, then the “No DBI” column should be used for Read Latency. When MR3 OP[6]=1_B, then the “w/DBI” column should be used for Read Latency.
 - Write Latency Set “A” and Set “B” is determined by MR2 OP[6]. When MR2 OP[6]=0_B, then Write Latency Set “A” should be used. When MR2 OP[6]=1_B, then Write Latency Set “B” should be used.
 - The programmed value of nWR is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto precharge). It is determined by RU(tWR/tCK).
 - The programmed value of nRTP is the number of clock cycles the LPDDR4x device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (auto precharge). It is determined by RU(tRTP/tCK).
 - nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

MR2_Device Feature 2 (MA<7:0> = 02_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|-----|-----|-----|-----|-----|-----|-----|
| WR Lev | WLS | WL | | | RL | | |

| Function | Register Type | Operand | Data | Notes |
|----------------------------|---------------|---------|---|-------|
| RL (Read latency) | Write only | OP[2:0] | RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0_B) 000_B : RL=6, nRTP=8 (Default) 001_B : RL=10, nRTP=8 010_B : RL=14, nRTP=8 011_B : RL=20, nRTP=8 100_B : RL=24, nRTP=10 101_B : RL=28, nRTP=12 110_B : RL=32, nRTP=14 111_B : RL=36, nRTP=16 RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1_B) 000_B : RL= 6, nRTP=8 001_B : RL= 12, nRTP=8 010_B : RL= 16, nRTP=8 011_B : RL= 22, nRTP=8 100_B : RL= 28, nRTP=10 101_B : RL= 32, nRTP=12 110_B : RL= 36, nRTP=14 111_B : RL= 40, nRTP=16 | 1,3,4 |
| WL (Write latency) | | OP[5:3] | WL Set "A" (MR2 OP[6]=0_B) 000_B : WL=4 (Default) 001_B : WL=6 010_B : WL=8 011_B : WL=10 100_B : WL=12 101_B : WL=14 110_B : WL=16 111_B : WL=18 WL Set "B" (MR2 OP[6]=1_B) 000_B : WL=4 001_B : WL=8 010_B : WL=12 011_B : WL=18 100_B : WL=22 101_B : WL=26 110_B : WL=30 111_B : WL=34 | 1,3,4 |
| WLS (Write latency set) | | OP[6] | 0_B : WL Set "A" (default) 1_B : WL Set "B" | 1,3,4 |
| WR Leveling | | OP[7] | 0_B : Disabled (default) 1_B : Enabled | 2 |

- NOTE :**
- 1) See Latency Code Frequency Table for allowable frequency ranges for RL/WL/nWR/nRTP.
 - 2) After a MRW to set the Write Leveling Enable bit (OP[7]=1_B), the LPDDR4x device remains in the MRW state until another MRW command clears the bit (OP[7]=0_B). No other commands are allowed until the Write Leveling Enable bit is cleared.
 - 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - 4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR3_I/O Configuration 1 (MA<7:0> = 03_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------|------|-----|-----|------|--------|--------|
| DBI-WR | DBI-RD | PDDS | | | PPRP | WR PST | PU-CAL |

| Function | Register Type | Operand | Data | Notes |
|---------------------------------------|---------------|---------|---|-------|
| PU-Cal (Pull-up Calibration Point) | Write only | OP[0] | 0_B : V _{DDQ} *0.6 1_B : V _{DDQ} *0.5 (default) | 1,4 |
| WR PST (WR Post-Amble Length) | | OP[1] | 0_B : WR Post-amble = 0.5*tCK (default) 1_B : WR Post-amble = 1.5*tCK (Vendor specific function) | 2,3,5 |
| Post Package Repair Protection | | OP[2] | 0_B : PPR protection disabled (default) 1_B : PPR protection enabled | 6 |
| PDDS (Pull-Down Drive Strength) | | OP[5:3] | 000_B : RFU 001_B : RZQ/1 010_B : RZQ/2 011_B : RZQ/3 100_B : RZQ/4 101_B : RZQ/5 110_B : RZQ/6 (default) 111_B : Reserved | 1,2,3 |
| DBI-RD (DBI-Read Enable) | | OP[6] | 0_B : Disabled (default) 1_B : Enabled | 2,3 |
| DBI-WR (DBI-Write Enable) | | OP[7] | 0_B : Disabled (default) 1_B : Enabled | 2,3 |

NOTE :

- 1) All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
- 2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
- 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- 4) For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
- 5) Refer to the supplier data sheet for vendor specific function. 1.5*tCK apply > 1.6GHz clock.
- 6) If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset. MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

MR4_Refresh rate (MA<7:0> = 04_H)

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----|----------------|-----|------|----------|--------------|-----|-----|
| TUF | Thermal Offset | | PPRE | SR Abort | Refresh Rate | | |

| Function | Register Type | Operand | Data | Notes |
|--|---------------|---------|--|------------------|
| Refresh Rate | Read-only | OP[2:0] | 00_B : SDRAM Low temperature operating limit exceeded 001_B : 4x refresh 010_B : 2x refresh 011_B : 1x refresh (default) 100_B : 0.5x refresh 101_B : 0.25x refresh, no de-rating 110_B : 0.25x refresh, with de-rating 111_B : SDRAM High temperature operating limit exceeded | 1,2,3,4 7,8,9 |
| SR Abort (Self Refresh Abort) | Write-only | OP[3] | 0_B : Disable (default) 1_B : Enable | 9,11 |
| PPRE (Post-package repair entry/exit) | Write-only | OP[4] | 0_B : Exit PPR mode (default) 1_B : Enter PPR mode | 5,9 |
| Thermal Offset (Vendor Specific Function) | Write-only | OP[6:5] | 00_B : No offset, 0~5°C gradient (default) 01_B : 5°C offset, 5~10°C gradient 10_B : 10°C offset, 10~15°C gradient 11_B : Reserved | 10 |
| TUF (Temperature Update Flag) | Read-only | OP[7] | 0_B : No change in OP[2:0] since last MR4 read (default) 1_B : Change in OP[2:0] since last MR4 read | 6,7,8 |

- NOTE :**
- 1) The refresh rate for each MR4 OP[2:0] setting applies to tREFI, tREFIpb and tREFW. OP[2:0]=011_B corresponds to a device temperature of 85°C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1_B, the device temperature is greater than 85°C.
 - 2) At higher temperatures (>85°C), AC timing derating may be required. If derating is required the LPDDR4x will set OP[2:0]=110_B. See derating timing requirements in the AC Timing section.
 - 3) DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
 - 4) The device may not operate properly when OP[2:0]=000_B or 111_B.
 - 5) Post-package repair can be entered or exited by writing to OP[4].
 - 6) When OP[7]=1_B, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
 - 7) OP[7]=0_B at power-up. OP[2:0] bits are valid after initialization sequence (Te).
 - 8) See the section on "Temperature Sensor" for information on the recommended frequency of reading MR4.
 - 9) OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
 - 10) Refer to the supplier data sheet for vendor specific function.

MR5_Basic Configuration 1 (MA<7:0> = 05_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|
| LPDDR4x Manufacturer ID | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-------------------------|---------------|---------|------------------------------|-------|
| LPDDR4x Manufacturer ID | Read-only | OP[7:0] | 0000 0001_B | |

MR6_Basic Configuration 2 (MA<7:0> = 06_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID-1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-----------------------|---------------|---------|--|-------|
| LPDDR4x Revision ID-1 | Read-only | OP[7:0] | 0000 1000_B : l-version | 1 |

- NOTE :**
- 1) MR6 is vendor specific.

MR7_Basic Configuration 3 (MA<7:0> = 07_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---------------|-----|-----|-----|-----|-----|-----|-----|
| Revision ID-2 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-----------------------|---------------|---------|-----------------------------|-------|
| LPDDR4x Revision ID-2 | Read-only | OP[7:1] | 0000 000_B | 1 |

NOTE :
1) MR7 is vendor specific.

MR8_Basic Configuration 4 (MA<7:0> = 08_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-----------|-----|---------|-----|-----|-----|------|-----|
| I/O width | | Density | | | | Type | |

| Function | Register Type | Operand | Data | Notes |
|-----------|---------------|---------|---|-------|
| Type | Read-only | OP[1:0] | 00_B : LPDDR4 S16 SDRAM (16n pre-fetch) Standard VDDQ(1.1V) only 10_B : LPDDR4x S16 SDRAM (16n pre-fetch) LOW VDDQ(0.6V) only All Others : Reserved | |
| Density | | OP[5:2] | 0000_B : 4Gb dual channel die / 2Gb single channel die 0001_B : 6Gb dual channel die / 3Gb single channel die 0010_B : 8Gb dual channel die / 4Gb single channel die 0011_B : 12Gb dual channel die / 6Gb single channel die 0100_B : 16Gb dual channel die / 8Gb single channel die 0101_B : 24Gb dual channel die / 12Gb single channel die 0110_B : 32Gb dual channel die / 16Gb single channel die All Others : Reserved | |
| I/O width | | OP[7:6] | 00_B : x16 (per channel) All Others : Reserved | |

MR9_Test Mode (MA<7:0> = 09_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------------|-----|-----|-----|-----|-----|-----|-----|
| Vendor-specific Test Register | | | | | | | |

NOTE :
1) Only 00_H should be written to this register.

MR10_IO Calibration (MA<7:0> = 0A_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----|-----|-----|-----|-----|-----|----------|
| (RFU) | | | | | | | ZQ-Reset |

| Function | Register Type | Operand | Data | Notes |
|----------|---------------|---------|--|-------|
| ZQ-Reset | Write-only | OP[0] | 0_B : Normal Operation (Default) 1_B : ZQ Reset | 1,2 |

NOTE :
1) See the AC Timing tables for calibration latency and timing
2) If the ZQ-pin is connected to VDDQ through RZQ, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to VSS, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR11_ODT Feature (MA<7:0> = 0B_H):

| | | OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--|---------------|---------|--|-----|-----|-------|--------|-----|-------|
| | | (RFU) | CA ODT | | | (RFU) | DQ ODT | | |
| Function | Register Type | Operand | Data | | | | | | Notes |
| DQ ODT (DQ Bus Receiver On-Die-Termination) | Write-only | OP[2:0] | 000_B : Disable (Default) 001_B : RZQ/1 010_B : RZQ/2 011_B : RZQ/3 100_B : RZQ/4 101_B : RZQ/5 110_B : RZQ/6 111_B : RFU | | | | | | 1,2,3 |
| CA ODT (CA Bus Receiver On-Die-Termination) | | OP[6:4] | 000_B : Disable (Default) 001_B : RZQ/1 010_B : RZQ/2 011_B : RZQ/3 100_B : RZQ/4 101_B : RZQ/5 110_B : RZQ/6 111_B : RFU | | | | | | 1,2,3 |

- NOTE :**
- 1) All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re.calibration may be required as voltage and temperature vary.
 - 2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR12_VREF(CA) Setting/Range (MA<7:0> = 0C_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-------|----------------------|-----|-----|-----|-----|-----|
| (RFU) | VR-CA | V _{REF(CA)} | | | | | |

| Function | Register Type | Operand | Data | Notes |
|--|---------------|---------|--|-----------|
| V _{REF(CA)} (V _{REF(CA)} Setting) | Read/Write | OP[5:0] | 000000_B : -- Thru . 110010_B : See table below All Others : Reserved | 1,2,3,5,6 |
| VR-CA (V _{REF(CA)} Range) | | OP[6] | 0_B : V _{REF(CA)} Range[0] enabled 1_B : V _{REF(CA)} Range[1] enabled (default) | 1,2,4,5,6 |

- NOTE :**
- 1) This register controls the V_{REF(CA)} levels.
 - 2) A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
 - 3) A write to OP[5:0] sets the internal V_{REF(CA)} level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF(CA)} to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF(CA)} training for more information.
 - 4) A write to OP[6] switches the LPDDR4x between two internal V_{REF(CA)} ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF(CA)} register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
 - 5) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - 6) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

[Table 13] V_{REF} Settings for Range[0] and Range[1]

| Function | Operand | Range[0] Values (% of V _{DDQ}) | | Range[1] Values (% of V _{DDQ}) | | Notes |
|--|-----------------------------------|--|-----------------------------------|--|---|-------|
| V _{REF} Settings for MR12 | OP[5:0] | 000000_B : 15.0% | 011010_B : 30.6% | 000000_B : 32.9% | 011010_B : 48.5% | 1,2,3 |
| | | 000001_B : 15.6% | 011011_B : 31.2% | 000001_B : 33.5% | 011011_B : 49.1% | |
| | | 000010_B : 16.2% | 011100_B : 31.8% | 000010_B : 34.1% | 011100_B : 49.7% | |
| | | 000011_B : 16.8% | 011101_B : 32.4% | 000011_B : 34.7% | 011101_B : 50.3% (Default) | |
| | | 000100_B : 17.4% | 011110_B : 33.0% | 000100_B : 35.3% | 011110_B : 50.9% | |
| | | 000101_B : 18.0% | 011111_B : 33.6% | 000101_B : 35.9% | 011111_B : 51.5% | |
| | | 000110_B : 18.6% | 100000_B : 34.2% | 000110_B : 36.5% | 100000_B : 52.1% | |
| | | 000111_B : 19.2% | 100001_B : 34.8% | 000111_B : 37.1% | 100001_B : 52.7% | |
| | | 001000_B : 19.8% | 100010_B : 35.4% | 001000_B : 37.7% | 100010_B : 53.3% | |
| | | 001001_B : 20.4% | 100011_B : 36.0% | 001001_B : 38.3% | 100011_B : 53.9% | |
| | | 001010_B : 21.0% | 100100_B : 36.6% | 001010_B : 38.9% | 100100_B : 54.5% | |
| | | 001011_B : 21.6% | 100101_B : 37.2% | 001011_B : 39.5% | 100101_B : 55.1% | |
| | | 001100_B : 22.2% | 100110_B : 37.8% | 001100_B : 40.1% | 100110_B : 55.7% | |
| | | 001101_B : 22.8% | 100111_B : 38.4% | 001101_B : 40.7% | 100111_B : 56.3% | |
| | | 001110_B : 23.4% | 101000_B : 39.0% | 001110_B : 41.3% | 101000_B : 56.9% | |
| | | 001111_B : 24.0% | 101001_B : 39.6% | 001111_B : 41.9% | 101001_B : 57.5% | |
| | | 010000_B : 24.6% | 101010_B : 40.2% | 010000_B : 42.5% | 101010_B : 58.1% | |
| | | 010001_B : 25.2% | 101011_B : 40.8% | 010001_B : 43.1% | 101011_B : 58.7% | |
| | | 010010_B : 25.8% | 101100_B : 41.4% | 010010_B : 43.7% | 101100_B : 59.3% | |
| | | 010011_B : 26.4% | 101101_B : 42.0% | 010011_B : 44.3% | 101101_B : 59.9% | |
| 010100_B : 27.0% | 101110_B : 42.6% | 010100_B : 44.9% | 101110_B : 60.5% | | | |
| 010101_B : 27.6% | 101111_B : 43.2% | 010101_B : 45.5% | 101111_B : 61.1% | | | |
| 010110_B : 28.2% | 110000_B : 43.8% | 010110_B : 46.1% | 110000_B : 61.7% | | | |
| 010111_B : 28.8% | 110001_B : 44.4% | 010111_B : 46.7% | 110001_B : 62.3% | | | |
| 011000_B : 29.4% | 110010_B : 45.0% | 011000_B : 47.3% | 110010_B : 62.9% | | | |
| 011001_B : 30.0% | All Others : Reserved | 011001_B : 47.9% | All Others : Reserved | | | |

- NOTE:**
- 1) These values may be used for MR12 OP[5:0] to set the V_{REF(CA)} levels in the LPDDR4x.
 - 2) The range may be selected in the MR12 register by setting OP[6] appropriately.
 - 3) The MR12 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

MR13_CBT,RPT,VRO,VRCG,RRO,DM_DIS,FSP-WR, FSP-OP (MA<7:0> = 0D_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------|-----|-----|------|-----|-----|-----|
| FSP-OP | FSP-WR | DMD | RRO | VRCG | VRO | RPT | CBT |

| Function | Register Type | Operand | Data | Notes |
|--|---------------|---------|--|-------|
| CBT (Command Bus Training) | Write-only | OP[0] | 0_B : Normal Operation (default) 1_B : Command Bus Training Mode Enabled | 1 |
| RPT (Read Preamble Training Mode) | | OP[1] | 0_B : Disable (default) 1_B : Enable | |
| VRO (V _{REF} Output) | | OP[2] | 0_B : Normal operation (default) 1_B : Output the V _{REF(CA)} and V _{REF(DQ)} values on DQ bits | 2 |
| VRCG (V _{REF} Current Generator) | | OP[3] | 0_B : Normal operation (default) 1_B : V _{REF} fast response (high current) mode | 3 |
| RRO (Refresh Rate Option) | | OP[4] | 0_B : Disable codes 001 and 010 in MR4 OP[2:0] 1_B : Enable all codes in MR4 OP[2:0] | 4,5 |
| DMD (Data Mask Disable) | | OP[5] | 0_B : Data Mask Operation Enabled (default) 1_B : Data Mask Operation Disabled | 6 |
| FSP-WR (Frequency Set Point Write/Read) | | OP[6] | 0_B : Frequency-Set-Point [0] (default) 1_B : Frequency-Set-Point [1] | 7 |
| FSP-OP (Frequency Set Point Operation Mode) | | OP[7] | 0_B : Frequency-Set-Point [0] (default) 1_B : Frequency-Set-Point [1] | 8 |

NOTE :

- 1) A write to set OP[0]=1_B causes the LPDDR4x to enter the Command Bus training mode. When OP[0]=1_B and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0_B) and return to normal operation. See the Command Bus Training section for more information.
- 2) When set, the LPDDR4x will output the V_{REF(CA)} and V_{REF(DQ)} voltages on DQ pins. Only the "active" frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal VREF levels. The DQ pins used for V_{REF} output are vendor specific.
- 3) When OP[3]=1_B, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
- 4) MR13 OP[4] RRO bit is valid only when MR0 OP[0]= 1_B. For LPDDR4x devices with MR0 OP[0] = 0_B, MR4 OP[2:0] bits are not dependent on MR13 OP4.
- 5) When OP[4] = 0_B, only 001_B and 010_B in MR4 OP[2:0] are disabled. LPDDR4x devices must report 011_B instead of 001_B or 010_B in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
- 6) When enabled (OP[5]=0_B) data masking is enabled for the device. When disabled (OP[5]=1_B), masked write command is illegal. See LPDDR4x Data Mask (DM) and Data Bus Inversion (DBI_{dc}) Function in operation timing datasheet.
- 7) FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V_{REF(CA)} Setting, V_{REF(CA)} Range, V_{REF(DQ)} Setting, V_{REF(DQ)} Range. For more information, refer to Frequency Set Point section in operations and timing spec.
- 8) FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V_{REF(CA)} Setting, V_{REF(CA)} Range, V_{REF(DQ)} Setting, V_{REF(DQ)} Range. For more information, refer to Frequency Set Point section in operations and timing spec.

MR14_VREF(DQ) Setting/Range (MA<7:0> = 0E_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|--------|----------------------|-----|-----|-----|-----|-----|
| (RFU) | VR(DQ) | V _{REF(DQ)} | | | | | |

| Function | Register Type | Operand | Data | Notes |
|--|---------------|---------|--|---------------|
| V _{REF(DQ)} (V _{REF(DQ)} Setting) | Read/Write | OP[5:0] | 000000_B : -- Thru . 110010_B : See table below All Others : Reserved | 1,2,3, 5,6 |
| V _{REF(DQ)} (V _{REF(DQ)} Range) | | OP[6] | 0_B : V _{REF(DQ)} Range [0] enabled 1_B : V _{REF(DQ)} Range [1] enabled (default) | 1,2,4, 5,6 |

- NOTE :**
- 1) This register controls the V_{REF(DQ)} levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(DQ)[1] may be selected by setting OP[6] appropriately.
 - 2) A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
 - 3) A write to OP[5:0] sets the internal V_{REF(DQ)} level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF(DQ)} to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF(DQ)} training for more information.
 - 4) A write to OP[6] switches the LPDDR4x between two internal V_{REF(DQ)} ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF(DQ)} register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
 - 5) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - 6) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

[Table 14] VREF Settings for Range[0] and Range[1]

| Function | Operand | Range[0] Values (%of VDDQ) | | Range[1] Values (%of VDDQ) | | Notes |
|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|---|-------|
| VREF Settings for MR14 | OP[5:0] | 000000_B : 15.0% | 011010_B : 30.6% | 000000_B : 32.9% | 011010_B : 48.5% | 1,2,3 |
| | | 000001_B : 15.6% | 011011_B : 31.2% | 000001_B : 33.5% | 011011_B : 49.1% | |
| | | 000010_B : 16.2% | 011100_B : 31.8% | 000010_B : 34.1% | 011100_B : 49.7% | |
| | | 000011_B : 16.8% | 011101_B : 32.4% | 000011_B : 34.7% | 011101_B : 50.3% (Default) | |
| | | 000100_B : 17.4% | 011110_B : 33.0% | 000100_B : 35.3% | 011110_B : 50.9% | |
| | | 000101_B : 18.0% | 011111_B : 33.6% | 000101_B : 35.9% | 011111_B : 51.5% | |
| | | 000110_B : 18.6% | 100000_B : 34.2% | 000110_B : 36.5% | 100000_B : 52.1% | |
| | | 000111_B : 19.2% | 100001_B : 34.8% | 000111_B : 37.1% | 100001_B : 52.7% | |
| | | 001000_B : 19.8% | 100010_B : 35.4% | 001000_B : 37.7% | 100010_B : 53.3% | |
| | | 001001_B : 20.4% | 100011_B : 36.0% | 001001_B : 38.3% | 100011_B : 53.9% | |
| | | 001010_B : 21.0% | 100100_B : 36.6% | 001010_B : 38.9% | 100100_B : 54.5% | |
| | | 001011_B : 21.6% | 100101_B : 37.2% | 001011_B : 39.5% | 100101_B : 55.1% | |
| | | 001100_B : 22.2% | 100110_B : 37.8% | 001100_B : 40.1% | 100110_B : 55.7% | |
| | | 001101_B : 22.8% | 100111_B : 38.4% | 001101_B : 40.7% | 100111_B : 56.3% | |
| | | 001110_B : 23.4% | 101000_B : 39.0% | 001110_B : 41.3% | 101000_B : 56.9% | |
| | | 001111_B : 24.0% | 101001_B : 39.6% | 001111_B : 41.9% | 101001_B : 57.5% | |
| | | 010000_B : 24.6% | 101010_B : 40.2% | 010000_B : 42.5% | 101010_B : 58.1% | |
| | | 010001_B : 25.2% | 101011_B : 40.8% | 010001_B : 43.1% | 101011_B : 58.7% | |
| | | 010010_B : 25.8% | 101100_B : 41.4% | 010010_B : 43.7% | 101100_B : 59.3% | |
| | | 010011_B : 26.4% | 101101_B : 42.0% | 010011_B : 44.3% | 101101_B : 59.9% | |
| 010100_B : 27.0% | 101110_B : 42.6% | 010100_B : 44.9% | 101110_B : 60.5% | | | |
| 010101_B : 27.6% | 101111_B : 43.2% | 010101_B : 45.5% | 101111_B : 61.1% | | | |
| 010110_B : 28.2% | 110000_B : 43.8% | 010110_B : 46.1% | 110000_B : 61.7% | | | |
| 010111_B : 28.8% | 110001_B : 44.4% | 010111_B : 46.7% | 110001_B : 62.3% | | | |
| 011000_B : 29.4% | 110010_B : 45.0% | 011000_B : 47.3% | 110010_B : 62.9% | | | |
| 011001_B : 30.0% | All Others : Reserved | 011001_B : 47.9% | All Others : Reserved | | | |

- NOTE:**
- 1) These values may be used for MR14 OP[5:0] to set the V_{REF(DQ)} levels in the LPDDR4x.
 - 2) The range may be selected in the MR14 register by setting OP[6] appropriately.
 - 3) The MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and un-terminated operation, or between different high-frequency setting which may use different terminations values.

MR15_Lower-Byte Invert for DQ Calibration (MA<7:0> = 0F_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|-----|-----|-----|-----|-----|-----|-----|
| Lower-Byte Invert Register for DQ Calibration | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|--------------------------------------|---------------|---------|---|-------|
| Lower-Byte Invert for DQ Calibration | Write-only | OP[7:0] | The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0_B : Do not invert 1_B : Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55 _H | 1,2,3 |

- NOTE :**
- 1) This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR15 OP[7:0]=00010101_B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
 - 2) DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
 - 3) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

[Table 15] MR15 Invert Register Pin Mapping

| PIN | DQ0 | DQ1 | DQ2 | DQ3 | DMI0 | DQ4 | DQ5 | DQ6 | DQ7 |
|------|-----|-----|-----|-----|-----------|-----|-----|-----|-----|
| MR15 | OP0 | OP1 | OP2 | OP3 | NO-Invert | OP4 | OP5 | OP6 | OP7 |

MR16_PASR_Bank Mask (MA<7:0> = 010_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------------|-----|-----|-----|-----|-----|-----|-----|
| PASR Bank Mask | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-----------------|---------------|---------|---|-------|
| Bank [7:0] Mask | Write-only | OP[7:0] | 0_B : Bank Refresh Enabled (default) : Unmasked 1_B : Bank Refresh disabled : Masked | 1 |

| OP | Bank Mask | 8-Bank SDRAM |
|----|-----------|--------------|
| 0 | XXXXXXX1 | Bank 0 |
| 1 | XXXXXX1X | Bank 1 |
| 2 | XXXXX1XX | Bank 2 |
| 3 | XXXX1XXX | Bank 3 |
| 4 | XXX1XXXX | Bank 4 |
| 5 | XX1XXXXX | Bank 5 |
| 6 | X1XXXXXX | Bank 6 |
| 7 | 1XXXXXXX | Bank 7 |

- NOTE :**
- 1) When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
 - 2) PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

MR17_PASR Segment Mask (MA<7:0> = 011_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------|-----|-----|-----|-----|-----|-----|-----|
| PASR Segment Mask | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-------------------|---------------|---------|---|-------|
| PASR Segment Mask | Write-only | OP[7:0] | 0_B : Segment Refresh enabled (default) 1_B : Segment Refresh disabled | |

| Segment | OP | Segment Mask | 2Gb | 3Gb | 4Gb | 6Gb | 8Gb | 12Gb | 16Gb | |
|---------|----|--------------|------------------------|--------------------|------------------------|--------------------|------------------------|--------------------|------------------------|--|
| | | | per channel | per channel | per channel | per channel | per channel | per channel | per channel | |
| | | | R13:11 | R14:12 | R14:12 | R15:13 | R15:13 | R16:14 | R16:14 | |
| 0 | 0 | XXXXXXXX1 | 000_B | | | | | | | |
| 1 | 1 | XXXXXX1X | 001_B | | | | | | | |
| 2 | 2 | XXXXX1XX | 010_B | | | | | | | |
| 3 | 3 | XXXX1XXX | 011_B | | | | | | | |
| 4 | 4 | XXX1XXXX | 100_B | | | | | | | |
| 5 | 5 | XX1XXXXX | 101_B | | | | | | | |
| 6 | 6 | X1XXXXXX | 110_B | Not Allowed | 110_B | Not Allowed | 110_B | Not Allowed | 110_B | |
| 7 | 7 | 1XXXXXXX | 111_B | | 111_B | | 111_B | | 111_B | |

NOTE :

- 1) This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular segment.
- 2) PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.
- 3) For 3Gb, 6Gb, and 12Gb per channel densities, OP[7:6] must always be LOW (=00B).

MR18_IT-LSB (MA<7:0> = 12_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS Oscillator Count-LSB | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---------------|---------|-------------------------------------|-------|
| DQS Oscillator (WR Training DQS Oscillator) | Read-only | OP[7:0] | 0-255 LSB DRAM DQS Oscillator Count | 1,2,3 |

NOTE :

- 1) MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
- 2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
- 3) A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR19_IT-MSB (MA<7:0> = 13_H) :

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS Oscillator Count-MSB | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---------------|---------|-------------------------------------|-------|
| DQS Oscillator (WR Training DQS Oscillator) | Read-only | OP[7:0] | 0-255 MSB DRAM DQS Oscillator Count | 1,2,3 |

NOTE :

- 1) MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
- 2) Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
- 3) A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR20_Upper-Byte Invert for DQ Calibration (MA<7:0> = 14_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|-----|-----|-----|-----|-----|-----|-----|
| Upper-Byte Invert Register for DQ Calibration | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|--------------------------------------|---------------|---------|--|-------|
| Upper-Byte Invert for DQ Calibration | Write-only | OP[7:0] | The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0_B : Do not invert 1_B : Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55 _H | 1,2 |

NOTE:

- 1) This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combination of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
- 2) DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
- 3) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

[Table 16] MR20 Invert Register Pin Mapping

| PIN | DQ8 | DQ9 | DQ10 | DQ11 | DMI1 | DQ12 | DQ13 | DQ14 | DQ15 |
|------|-----|-----|------|------|-----------|------|------|------|------|
| MR20 | OP0 | OP1 | OP2 | OP3 | NO-Invert | OP4 | OP5 | OP6 | OP7 |

MR21_Low Speed CA Buffer (MA<7:0> = 015_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----|---------------------|-------|-----|-----|-----|-----|
| (RFU) | | Low Speed CA buffer | (RFU) | | | | |

| Function | Register Type | Operand | Data | Notes |
|---------------------|---------------|---------|---|---------------|
| Low Speed CA Buffer | Write-only | OP[5] | 0_B : Normal CA Buffer (Default) 1_B : Low Speed CA Buffer | 1,2,3,4,5,6,7 |

- 1) Support for the Low Speed CA Buffer feature enabled by MR21 OP[5] is optional. Refer to manufacturer data sheet for availability.
- 2) Low Speed CA Buffer feature can enable lower power for some manufacturers' designs. The maximum clock speed for this mode is vendor-specific, but is not above 800 MHz. Refer to manufacturer data sheet for details.
- 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
- 4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
- 5) After completing all the other MRW commands to set the values besides MR21 OP[5] setting, MR21 OP[5] can be enabled to "High". Low Power CA Buffer cannot be enabled prior to full device initialization (completion of Step 9 in power up sequence).
- 6) Low speed CA buffer is allowed to be enabled only when CA ODT is disabled.
- 7) SDRAM not supporting Low Speed CA Buffer will ignore MR21 OP[5] setting.

MR22_ODT Feature (MA<7:0> = 16_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----|---------|---------|---------|---------|-----|-----|
| (RFU) | | ODTD-CA | ODTE-CS | ODTE-CK | SoC ODT | | |

| Function | Register Type | Operand | Data | Notes |
|---|---------------|---------|--|-------|
| SoC ODT (Controller ODT Value for VOH calibration) | Write-only | OP[2:0] | 000_B : Disable (Default) 001_B : RZQ/1 (illegal if MR3 OP0=0 _B) 010_B : RZQ/2 011_B : RZQ/3 (illegal if MR3 OP0=0 _B) 100_B : RZQ/4 101_B : RZQ/5 (illegal if MR3 OP0=0 _B) 110_B : RZQ/6 (illegal if MR3 OP0=0 _B) 111_B : RFU | 1,2,3 |
| ODT-CK | | OP[3] | ODT bond PAD is ignored 0_B : ODT-CK Enabled (Default) 1_B : ODT-CK Disabled | 2,3,4 |
| ODT-CS | | OP[4] | ODT bond PAD is ignored 0_B : ODT-CS Enabled (Default) 1_B : ODT-CS Disabled | 2,3,4 |
| ODTD-CA (CA ODT termination disable) | | OP[5] | ODT bond PAD is ignored 0_B : ODT-CA Obeyes ODT_CA bond pad (default) 1_B : ODT-CA Disabled | 2,3,4 |

- NOTE :**
- 1) All values are "typical".
 - 2) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
 - 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
 - 4) LPDDR4x device ignore ODT bond PAD

[Table 17] DRAM PU strength & SoC ODT relation

| VOH CAL (MR3 OP0) | | SoC ODT Value (MR22 OP[2:0]) | | | | | | | |
|----------------------------------|--------------|------------------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| | | 000 _B | 001 _B | 010 _B | 011 _B | 100 _B | 101 _B | 110 _B | 111 _B |
| 0 _B (VOH=VDDQ*3/5) | SoC ODT | Disable | illegal | RZQ/ 2=120ohm | illegal | RZQ/ 4=60ohm | illegal | illegal | RFU |
| | DRAM Pull-up | Default | N/A | RZQ/ 3=80ohm | N/A | RZQ/ 6=40ohm | N/A | N/A | RFU |
| 1 _B (VOH=VDDQ/2) | SoC ODT | Disable | RZQ/ 1=240ohm | RZQ/ 2=120ohm | RZQ/ 3=80ohm | RZQ/ 4=60ohm | RZQ/ 5=48ohm | RZQ/ 6=40ohm | RFU |
| | DRAM Pull-up | Default | RZQ/ 1=240ohm | RZQ/ 2=120ohm | RZQ/ 3=80ohm | RZQ/ 4=60ohm | RZQ/ 5=48ohm | RZQ/ 6=40ohm | RFU |

A) There is no corresponding RZQ/x value for 001_B,011_B,101_B,110_B when MR3 OP0 = 0_B to support 3/5 VDDQ VOH value.

MR23_DQS Interval Timer Run Time (MA<7:0> = 17_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------------------------------------|-----|-----|-----|-----|-----|-----|-----|
| DQS interval timer run time setting | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-----------------------------|---------------|---------|--|-------|
| DQS interval timer run time | Write-only | OP[7:0] | 00000000_B : DQS interval timer stop via MPC Command (Default) 00000001_B : DQS timer stops automatically at 16 th clocks after timer start 00000010_B : DQS timer stops automatically at 32 nd clocks after timer start 00000011_B : DQS timer stops automatically at 48 th clocks after timer start 00000100_B : DQS timer stops automatically at 64 th clocks after timer start ----- Thru ----- 00111111_B : DQS timer stops automatically at (63X16) th clocks after timer start 01XXXXXX_B : DQS timer stops automatically at 2048 th clocks after timer start 10XXXXXX_B : DQS timer stops automatically at 4096 th clocks after timer start 11XXXXXX_B : DQS timer stops automatically at 8192 nd clocks after timer start | 1,2 |

NOTE :

- 1) MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000_B.
- 2) MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

MR24_TRR (MA<7:0> = 18_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|----------|--------------|-----|-----|---------------|-----------|-----|-----|
| TRR Mode | TRR mode BAn | | | Unlimited MAC | MAC Value | | |

| Function | Register Type | Operand | Data | Notes |
|---------------|---------------|---------|---|---|
| MAC Value | Read-only | OP[2:0] | 000_B : Unknown when bit OP3 =0 ¹⁾ Unlimited when bit OP3=1 ²⁾ 001_B : 700K 010_B : 600K 011_B : 500K 100_B : 400K 101_B : 300K 110_B : 200K 111_B : Reserved | |
| Unlimited MAC | | | OP[3] | 0_B : OP[2:0] define MAC value 1_B : Unlimited MAC value ^{2), 3)} |
| TRR Mode BAn | Write-only | OP[6:4] | 000_B : Bank 0 001_B : Bank 1 010_B : Bank 2 011_B : Bank 3 100_B : Bank 4 101_B : Bank 5 110_B : Bank 6 111_B : Bank 7 | |
| TRR Mode | | | OP[7] | 0_B : Disabled (default) 1_B : Enabled |

NOTE :

- 1) Unknown means that the device is not tested for tMAC and pass/fail values are unknown.
- 2) There is no restriction to number of activates.
- 3) MR24 OP [2:0] is set to ZERO.

MR25_PPR Resources (MA<7:0> = 19_H):

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------|--------|--------|--------|--------|--------|--------|--------|
| Bank 7 | Bank 6 | Bank 5 | Bank 4 | Bank 3 | Bank 2 | Bank 1 | Bank 0 |

| Function | Register Type | Operand | Data | Notes |
|--------------|---------------|---------|--|-------|
| PPR Resource | Read-only | OP[7:0] | 0_B : PPR Resource is not available 1_B : PPR Resource is available | |

MR26-29_(RFU) (MA<7:0> = 1A_H - 1D_H):
MR30_Reserved for Testing (MA<7:0> = 1E_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Valid 0 or 1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-------------------|---------------|---------|------------|-------|
| SDRAM will ignore | Write-only | OP[7:0] | Don't care | 1 |

NOTE :
 1) This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR31_(RFU) (MA<7:0> = 1F_H):
MR32_DQ Calibration Pattern A (MA<7:0>=20_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|-----|-----|-----|-----|-----|-----|-----|
| DQ Calibration Pattern "A" (default = 5A _H) | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---------------|---------|---|-------|
| Return DQ Calibration Pattern MR32 + MR40 | Write | OP[7:0] | X_B : An MPC command with OP[6:0]=1000011 _B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "5A _H " is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information) | |

MR33:38_(Do Not Use) (MA<7:0> = 21_H-26_H):
MR39_Reserved for Testing (MA<7:0> = 27_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|--------------|-----|-----|-----|-----|-----|-----|-----|
| Valid 0 or 1 | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|-------------------|---------------|---------|------------|-------|
| SDRAM will ignore | Write-only | OP[7:0] | Don't care | 1 |

NOTE :
 1) This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR40_DQ Calibration Pattern B (MA<7:0>=28_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|---|-----|-----|-----|-----|-----|-----|-----|
| DQ Calibration Pattern "B" (default = 3C _H) | | | | | | | |

| Function | Register Type | Operand | Data | Notes |
|---|---------------|---------|--|-------|
| Return DQ Calibration Pattern MR32 + MR40 | Write-only | OP[7:0] | X_B : A default pattern "3C _H " is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32, for more information. | 1,2,3 |

- NOTE :**
- 1) The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H, then the first bit transmitted will be a '1', followed by '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.
 - 2) MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR22 for more information. Data is never inverted on the DMI[1:0] pins.
 - 3) The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3 OP[6].
 - 4) No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3 OP[6].

MR41:47_ (Do Not Use)(MA<7:0> = 29_H-2F_H):
MR48:50_(RFU) (MA<7:0> = 30_H - 32_H):
MR51_Single Ended RDQS, WDQS, Clock (MA<7:0> = 33_H):

| OP7 | OP6 | OP5 | OP4 | OP3 | OP2 | OP1 | OP0 |
|-------|-----|-----|-----|--------------------|-------------------|-------------------|-------|
| (RFU) | | | | Single ended Clock | Single ended WDQS | Single ended RDQS | (RFU) |

| Function | Register Type | Operand | Data | Notes |
|--------------------|---------------|---------|---|------------|
| Single ended RDQS | Write-only | OP[1] | 0_B : Differential Read DQS (Default) 1_B : Single ended Read DQS | 1,2,3,4,5, |
| Single ended WDQS | | OP[2] | 0_B : Differential Write DQS (Default) 1_B : Single ended Write DQS | 1,2,3,4,6, |
| Single ended Clock | | OP[3] | 0_B : Differential Clock (Default), CK_t /CK_c 1_B : Single ended Clock, Only CK_t | 1,2,3,4,7 |

- NOTE :**
- 1) The features described in MR51 are optional. Please check the vendor for the availability.
 - 2) Device support for single ended mode features (MR51 OP[3:1]) is indicated in MR0 OP[5]
 - 3) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address.
 - 4) There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
 - 5) When single ended RDQS mode is enabled (MR51 OP[1] = 1_B), DRAM drives Read DQSB low or Hi-Z.
 - 6) When single ended WDQS mode is enabled (MR51 OP[2] = 1_B), Write DQSB is required to be at a valid logic level. A valid Write DQSB signal will meet this requirement.
 - 7) When single ended Clock mode is enabled (MR51 OP[3] = 1_B), CK_c is required to be the valid level required to be at a valid logic level. A valid CK_c signal will meet this requirement.

When DRAM is operating with single-ended mode, both CLKB and write DQSB shall be on "Low" state at all times whereas read DQSB is always on "Hi-Z" state. Refer to the table below.

| | | Differential Mode | Single-Ended Mode |
|-----------|------|-------------------|-------------------|
| CLK | CLK | Valid | Valid |
| | CLKB | Valid | 0 |
| Write DQS | DQS | Valid | Valid |
| | DQSB | Valid | 0 |
| Read DQS | DQS | Valid | Valid |
| | DQSB | Valid | Hi-Z |

MR52:63_(RFU) (MA<7:0> = 34_H - 3F_H) :

5 TRUTH TABLES

Operation or timing that is not specified is illegal, and after such an event, in order to guarantee proper operation, the LPDDR4x device must be reset or power-cycled and then restarted through the specified initialization sequence before normal operation can continue. CKE signal has to be held High when the commands listed in the command truth table input.

[Table 18] Command truth table

| SDRAM Command | SDR Com- mand Pins | SDR CA pins (6) | | | | | | CK_t edge | Notes |
|---|-----------------------|-----------------|-----|-----|-----|-----|-----|-----------|-------------|
| | CS | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 | | |
| Deselect (DES) | L | X | | | | | | R1 | 1,2 |
| Multi-Purpose Command (MPC) | H | L | L | L | L | L | OP6 | R1 | 1,9 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |
| Precharge (PRE) (Per Bank, All Bank) | H | L | L | L | L | H | AB | R1 | 1,2,3,4 |
| | L | BA0 | BA1 | BA2 | V | V | V | R2 | |
| Refresh (REF) (Per Bank, All Bank) | H | L | L | L | H | L | AB | R1 | 1,2,3,4 |
| | L | BA0 | BA1 | BA2 | V | V | V | R2 | |
| Self Refresh Entry (SRE) | H | L | L | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Write-1 (WR-1) | H | L | L | H | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| Self Refresh Exit (SRX) | H | L | L | H | L | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Mask Write-1 (MWR-1) | H | L | L | H | H | L | L | R1 | 1,2,3,5,6,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| RFU | H | L | L | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Read-1 (RD-1) | H | L | H | L | L | L | BL | R1 | 1,2,3,6,7,9 |
| | L | BA0 | BA1 | BA2 | V | C9 | AP | R2 | |
| CAS-2 (Write-2, Mask Write-2, Read-2, MRR-2, MPC) | H | L | H | L | L | H | C8 | R1 | 1,8,9 |
| | L | C2 | C3 | C4 | C5 | C6 | C7 | R2 | |
| RFU | H | L | H | L | H | L | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| RFU | H | L | H | L | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Mode Register Write-1 (MRW-1) | H | L | H | H | L | L | OP7 | R1 | 1,11 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| Mode Register Write-2 (MRW-2) | H | L | H | H | L | H | OP6 | R1 | 1,11 |
| | L | OP0 | OP1 | OP2 | OP3 | OP4 | OP5 | R2 | |
| Mode Register Read-1 (MRR-1) | H | L | H | H | H | L | V | R1 | 1,2,12 |
| | L | MA0 | MA1 | MA2 | MA3 | MA4 | MA5 | R2 | |
| RFU | H | L | H | H | H | H | V | R1 | 1,2 |
| | L | V | | | | | | R2 | |
| Activate-1 (ACT-1) | H | H | L | R12 | R13 | R14 | R15 | R1 | 1,2,3,10 |
| | L | BA0 | BA1 | BA2 | V | R10 | R11 | R2 | |
| Activate-2 (ACT-2) | H | H | H | R6 | R7 | R8 | R9 | R1 | 1,10 |
| | L | R0 | R1 | R2 | R3 | R4 | R5 | R2 | |

NOTE:

- 1) All LPDDR4x commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
- 2) "V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
- 3) Bank addresses BA[2:0] determine which bank is to be operated upon.
- 4) AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
- 5) Mask Write-1 command supports only BL 16. For Mask Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
- 6) AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an auto-precharge will occur to the bank associated with the Write, Mask Write or Read command.
- 7) If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
- 8) For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
- 9) Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or mode register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
- 10) Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
- 11) MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
- 12) MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

5.1 CKE Truth Tables

[Table 19] LPDDR4x : CKE Table 1), 2), 3), 4), 8)

| Device Current State | CKE _{n-1} | CKE _n | Command n | Operation | Device Next State | Notes |
|----------------------|--------------------|------------------|----------------------------------|---|-------------------|-------|
| Active Power Down | L | L | X | Maintain Active Power Down | Active Power Down | |
| | L | H | Deselect | Exit Active Power Down | Active | 5,6 |
| Idle Power Down | L | L | X | Maintain Idle Power Down | Idle Power Down | |
| | L | H | Deselect | Exit Idle Power Down | Idle | 5,6 |
| Self Refresh | L | L | X | Maintain power-down state within Self Refresh | Self Refresh | |
| | L | H | Deselect | Exit SREF power-down, enable command decode | Self Refresh | 5,6,7 |
| | H | L | Deselect | Enter SREF Power-Down, disable command decode | Self Refresh | 5,7 |
| | H | H | See Note 7 | See Note 7 | Self Refresh | 7 |
| Bank(s) Active | H | L | Deselect | Enter Active Power Down | Active Power Down | 5 |
| All Banks Idle | H | L | Deselect | Enter Idle Power Down | Idle Power Down | 5, 8 |
| Command Entry | H | H | Refer to the Command Truth Table | | | |

NOTE :

- 1) CKE is a strictly asynchronous input, and as such, has no relationship to CK.
- 2) "X" means "don't care."
- 3) "Current State" is the state of the LPDDR4x prior to a toggle of CKE.
- 4) "CKEn-1" is the logic state of CKE prior to a CKE toggle event, and "CKEn" is the state of CKE after the toggle event.
- 5) "Deselect" is the only valid command that can be present on the bus when CKE is toggled.
- 6) Power-Down exit time (tXP) should elapse before a command other than Deselect is issued. The clock must toggle at least twice during the tXP period, and must be stable before issuing a command.
- 7) When the device is in Self.Refresh, only MRR, MRW, or MPC commands are allowed. Certain restrictions apply to changing register contents via a MRW command during SREF. See MRW section for more information.
- 8) In the case of ODT disabled, all DQ output shall be Hi-Z. In the case of ODT enabled, all DQ shall be terminated to VSSQ.

5.2 State Truth Table

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all banks.

[Table 20] Current State Bank n - Command to Bank n

| Current State | Command | Operation | Next State | NOTES |
|---------------|--------------------|--|-----------------------|-----------|
| Any | NOP | Continue previous operation | Current State | |
| Idle | ACTIVATE | Select and activate row | Active | |
| | Refresh (Per Bank) | Begin to refresh | Refreshing (Per Bank) | 6 |
| | Refresh (All Bank) | Begin to refresh | Refreshing (All Bank) | 7 |
| | MRW | Write value to | MR Writing | 7 |
| | MRR | Read value from | Idle MR Reading | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8, 13 |
| Row Active | Read | Select column, and start read burst | Reading | 10 |
| | Write | Select column, and start write burst | Writing | 10 |
| | MRR | Read value from | Active MR Reading | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Reading | Read | Select column, and start new read burst | Reading | 9, 10 |
| | Write | Select column, and start write burst | Writing | 9, 10, 11 |
| Writing | Write | Select column, and start new write burst | Writing | 9, 10 |
| | Read | Select column, and start read burst | Reading | 9, 10, 12 |

NOTE :

- 1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XS}R or t_{XP} has been met if the previous state was Self Refresh or Power Down.
- 2) All states and sequences not shown are illegal or reserved.
- 3) Current State Definitions:
 - Idle: The bank or banks have been precharged, and t_{RP} has been met.
 - Active: A row in the bank has been activated, and t_{RCD} has been met. No data bursts / accesses and no register accesses are in progress.
 - Reading: A Read burst has been initiated, with Auto Precharge disabled.
 - Writing: A Write burst has been initiated, with Auto Precharge disabled.
- 4) The following states must not be interrupted by a command issued to the same bank. NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other banks are determined by its current state and , and according to .
 - Precharging: starts with the registration of a Precharge command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
 - Row Activating: starts with registration of an Activate command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the 'Active' state.
 - Read with AP Enabled: starts with the registration of the Read command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} has been met, the bank will be in the idle state.
 - Write with AP Enabled: starts with registration of a Write command with Auto Precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.
- 5) The following states must not be interrupted by any executable command; NOP commands must be applied to each positive clock edge during these states.
 - Refreshing (Per Bank): starts with registration of a Refresh (Per Bank) command and ends when t_{RFCpb} is met. Once t_{RFCpb} is met, the bank will be in an 'idle' state.
 - Refreshing (All Bank): starts with registration of an Refresh (All Bank) command and ends when t_{RFCab} is met. Once t_{RFCab} is met, the device will be in an 'all banks idle' state.
 - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
 - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
 - Idle MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
 - Active MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Active state.
 - Precharging All: starts with the registration of a Precharge-All command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.
- 6) Bank-specific; requires that the bank is idle and no bursts are in progress.
- 7) Not bank-specific; requires that all banks are idle and no bursts are in progress.
- 8) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
- 9) A command other than NOP should not be issued to the same bank while a Read or Write burst with Auto Precharge is enabled.
- 10) The new Read or Write command could be Auto Precharge enabled or Auto Precharge disabled.
- 11) A Write command may be applied after the completion of the Read burst; burst terminates are not permitted.
- 12) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.
- 13) If a Precharge command is issued to a bank in the Idle state, t_{RP} shall still apply.

[Table 21] Current State Bank n - Command to Bank m

| Current State of Bank n | Command for Bank m | Operation | Next State for Bank m | NOTES |
|---|--------------------|---|--------------------------------------|---------|
| Any | NOP | Continue previous operation | Current State of Bank m | |
| Idle | Any | Any command allowed to Bank m | - | |
| Row Activating, Active, or Precharging | Activate | Select and activate row in Bank m | Active | 6 |
| | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| | MRR | Read value from | Idle MR Reading or Active MR Reading | 9,10, |
| Reading (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,12 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing/Masked Writing (Autoprecharge disabled) | Read | Select column, and start read burst from Bank m | Reading | 7,14 |
| | Write | Select column, and start write burst to Bank m | Writing | 7 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Reading with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7,13 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,12,13 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |
| Writing/Masked Writing with Autoprecharge | Read | Select column, and start read burst from Bank m | Reading | 7,13,14 |
| | Write | Select column, and start write burst to Bank m | Writing | 7,13 |
| | Activate | Select and activate row in Bank m | Active | |
| | Precharge | Deactivate row in bank or banks | Precharging | 8 |

- NOTE :**
- 1) The table applies when both CKEn-1 and CKEn are HIGH, and after t_{XSR} or t_{XP} has been met if the previous state was Self Refresh or Power Down.
 - 2) All states and sequences not shown are illegal or reserved.
 - 3) Current State Definitions:
 - Idle: The bank has been precharged, and TRP has been met.
 - Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
 - Reading: A Read burst has been initiated, with Auto Precharge disabled.
 - Writing: A Write burst has been initiated, with Auto Precharge disabled
 - 4) Refresh, Self-Refresh, and Mode register Write commands may only be issued when all bank are idle.
 - 5) The following states must not be interrupted by any executable command; NOP commands must be applied during each clock cycle while in these states:
 - Idle MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Idle state.
 - Active MR Reading: starts with the registration of a MRR command and ends when t_{MRR} has been met. Once t_{MRR} has been met, the bank will be in the Active state.
 - Idle MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Idle state.
 - Active MR Writing: starts with the registration of a MRW command and ends when t_{MRW} has been met. Once t_{MRW} has been met, the bank will be in the Active state.
 - 6) t_{RRD} must be met between Activate command to Bank n and a subsequent Activate command to Bank m. Additionally, in the case of multiple banks activated, t_{FAW} must be satisfied.
 - 7) Reads or Writes listed in the Command column include Reads and Writes with Auto Precharge enabled and Reads and Writes with Auto Precharge disabled.
 - 8) This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
 - 9) MRR is allowed during the Row Activating state (Row Activating starts with registration of an Activate command and ends when tRCD is met.)
 - 10) MRR is allowed during the Precharging state. (Precharging starts with registration of a Precharge command and ends when t_{RP} is met.)
 - 11) The next state for Bank m depends on the current state of Bank m (Idle, Row Activating, Precharging, or Active). The reader shall note that the state may be in transition when a MRR is issued. Therefore, if Bank m is in the Row Activating state and Precharging, the next state may be Active and Precharge dependent upon t_{RCD} and t_{RP} respectively.
 - 12) A Write command may be applied after the completion of the Read burst, burst terminates are not permitted.
 - 13) Read with auto precharge enabled or a Write with Auto Precharge enabled may be followed by any valid command to other banks provided that the timing restrictions described in the Precharge & Auto Precharge clarification table are followed.
 - 14) A Read command may be applied after the completion of the Write burst, burst terminates are not permitted.

6 ABSOLUTE MAXIMUM DC RATINGS

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

[Table 22] Absolute Maximum DC Ratings

| Parameter | Symbol | Min | Max | Units | Notes |
|---|------------------------------------|------|-----|-------|-------|
| V _{DD1} supply voltage relative to V _{SS} | V _{DD1} | -0.4 | 2.1 | V | 1 |
| V _{DD2} supply voltage relative to V _{SS} | V _{DD2} | -0.4 | 1.4 | V | 1 |
| V _{DDQ} supply voltage relative to V _{SSQ} | V _{DDQ} | -0.4 | 1.4 | V | 1 |
| Voltage on any ball except V _{DD1} relative to V _{SS} | V _{IN} , V _{OUT} | -0.4 | 1.4 | V | |
| Storage Temperature | T _{STG} | -55 | 125 | °C | 2 |

NOTE :

1) See Power Ramp for relationships between power supplies.

2) Storage Temperature is the case surface temperature on the center/top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2 standard.

7 AC & DC OPERATING CONDITIONS

7.0 Recommended DC Operating Conditions

[Table 23] Recommended DC Operating Conditions

| Symbol | DRAM | LPDDR4x | | | Unit | Notes |
|--------|-----------------------------------|---------|------|------|------|-------|
| | | Min | Typ | Max | | |
| VDD1 | Core 1 Power | 1.70 | 1.80 | 1.95 | V | 1,2 |
| VDD2 | Core 2 Power / Input Buffer Power | 1.06 | 1.10 | 1.17 | V | 1,2,3 |
| VDDQ | I/O Buffer Power | 0.57 | 0.60 | 0.65 | V | 2,3 |

- NOTE :**
 1) VDD1 uses significantly less current than VDD2.
 2) The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
 3) The voltage noise tolerance from DC to 20MHz exceeding a pk-pk tolerance of 45mv at the DRAM ball is not included in the TdIVW.

7.1 Input Leakage Current

[Table 24] Input Leakage Current

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|-----------------------|--------|-----|-----|------|-------|
| Input Leakage current | I_L | -4 | 4 | uA | 1,2 |

- NOTE :**
 1) For CK_t, CK_c, CKE, CS, CA, ODT_CA and RESET_n. Any input $0V \leq V_{IN} \leq VDD2$ (All other pins not under test = 0V).
 2) CA ODT is disabled for CK_t, CK_c, CS, and CA.

7.2 Input/Output Leakage Current

| Parameter/Condition | Symbol | Min. | Max. | Unit | Notes |
|------------------------------|----------|------|------|------|-------|
| Input/Output Leakage current | I_{OZ} | -5 | 5 | uA | 1,2 |

- NOTE :**
 1) For DQ, DQS_t, DQS_c and DMI. Any I/O $0V \leq V_{OUT} \leq VDDQ$.
 2) I/Os status are disabled: High Impedance and ODT Off.

7.3 Operating Temperature Range

[Table 25] Operating Temperature Range

| Parameter/Condition | Symbol | Min | Max | Unit |
|---------------------|------------|-----|-----|------|
| Industrial | T_{OPER} | -40 | 95 | °C |

- NOTE :**
 1) Operating Temperature is the case surface temperature on the center top side of the LPDDR4x device. For the measurement conditions, please refer to JESD51-2.
 2) Either the device case temperature rating or the temperature sensor (See "Temperature Sensor" on [Command Definition & Timing Diagram]) may be used to set an appropriate refresh rate, determine the need for AC timing de-rating and/or monitor the operating temperature. When using the temperature sensor, the actual device case temperature may be higher than the T_{OPER} rating that applies for the Standard or Extended Temperature Ranges. For example, T_{CASE} may be above 85°C when the temperature sensor indicates a temperature of less than 85°C.

8 AC AND DC INPUT MEASUREMENT LEVELS

8.0 1.1V High speed LVCMOS (HS_LLVC MOS)

8.0.1 Standard specifications

All voltages are referenced to ground except where noted.

8.0.2 DC electrical characteristics

8.0.2.1 LPDDR4x Input Level for CKE

This definition applies to CKE_A/B.

[Table 26] LPDDR4x Input Level for CKE

| Parameter | Symbol | Min. | Max. | Unit | Note |
|-----------------------|--------------|-----------------------|-----------------------|------|------|
| Input high level (AC) | $V_{IH(AC)}$ | $0.75 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | 1 |
| Input low level (AC) | $V_{IL(AC)}$ | -0.2 | $0.25 \times V_{DD2}$ | V | 1 |
| Input high level (DC) | $V_{IH(DC)}$ | $0.65 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | |
| Input low level (DC) | $V_{IL(DC)}$ | -0.2 | $0.35 \times V_{DD2}$ | V | |

NOTE :

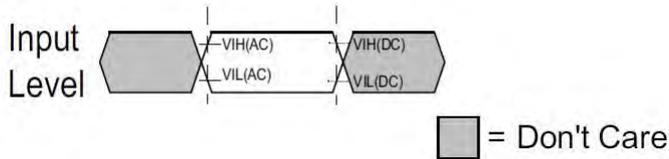


Figure 4. LPDDR4x Input AC timing definition for CKE

- 1) Refer LPDDR4x AC Over/Undershoot section.
 1-1). AC level is guaranteed transition point.
 1-2). DC level is hysteresis.

8.0.2.2 LPDDR4x Input Level for Reset_n and ODT_CA

This definition applies to Reset_n and ODT_CA.

[Table 27] LPDDR4x Input Level for Reset_n and ODT_CA

| Parameter | Symbol | Min. | Max. | Unit | Note |
|------------------|----------|-----------------------|-----------------------|------|------|
| Input high level | V_{IH} | $0.80 \times V_{DD2}$ | $V_{DD2} + 0.2$ | V | 1 |
| Input low level | V_{IL} | -0.2 | $0.20 \times V_{DD2}$ | V | 1 |

NOTE :

- 1) Refer LPDDR4x AC Over/Undershoot section.

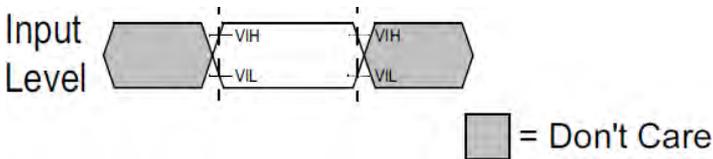


Figure 5. LPDDR4x Input AC timing definition for Reset_n and ODT_CA

8.1 AC Over/Undershoot

8.1.1 LPDDR4x AC Over/Undershoot

[Table 28] LPDDR4x AC Over/Undershoot

| Parameter | Specification |
|---|---------------|
| Maximum peak amplitude allowed for overshoot area. | 0.35V |
| Maximum peak amplitude allowed for undershoot area. | 0.35V |
| Maximum overshoot area above V_{DD}/V_{DDQ} . | 0.8V |
| Maximum undershoot area below V_{SS}/V_{SSQ} . | 0.8V |

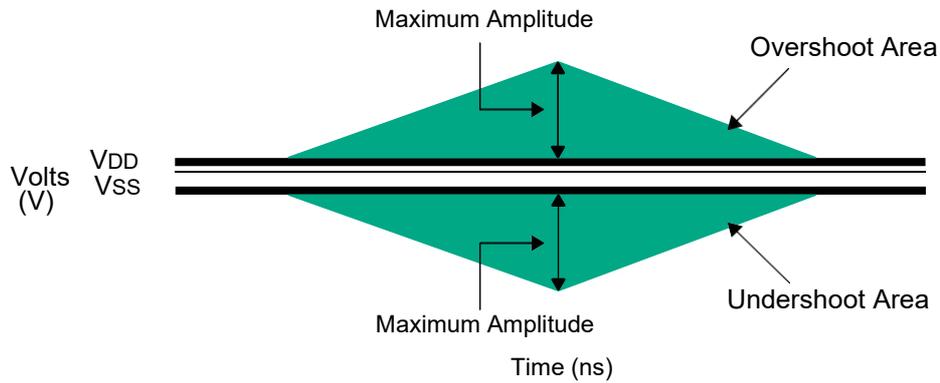


Figure 6. AC Overshoot and Undershoot Definition for Address and Control Pins

8.2 Differential Input Voltage

8.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both V_{indiff_CK} and $V_{indiff_CK}/2$ specification at input receiver and their measurement period is $1t_{CK}$. V_{indiff_CK} is the peak to peak voltage centered on 0 volts differential and $V_{indiff_CK}/2$ is max and min peak voltage from 0V.

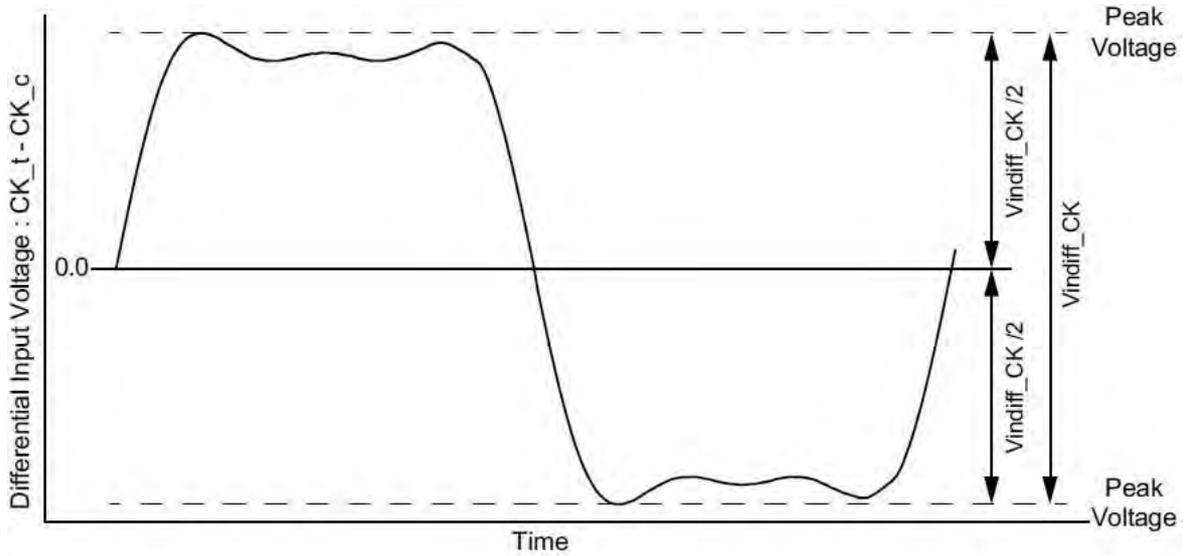


Figure 7. CK Differential Input Voltage

[Table 29] CK differential input voltage

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|-------------------------------|------------------|-------------------------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 ^{a)} | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| CK differential input voltage | V_{indiff_CK} | 420 | - | 380 | - | 360 | - | mV | 1 |

NOTE:

1) The peak voltage of Differential CK signals is calculated in a following equation.

$$V_{indiff_CK} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = V_{CK_t} - V_{CK_c}$$

a) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.2.2 Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in a following equation.

$$V_{IH.DIFF.PEAK \text{ Voltage}} = \text{Max}(f(t))$$

$$V_{IL.DIFF.PEAK \text{ Voltage}} = \text{Min}(f(t))$$

$$f(t) = V_{CK_t} - V_{CK_c}$$

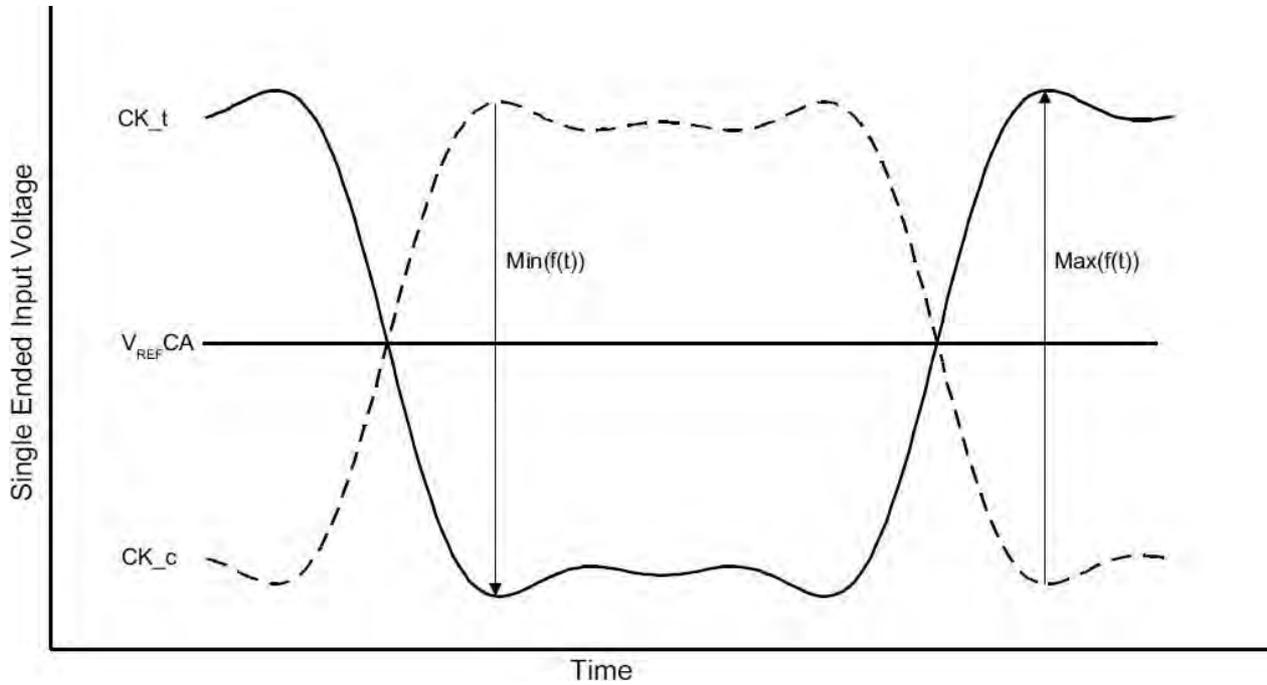


Figure 8. Definition of differential Clock Peak Voltage

NOTE:

1) VREFCA is LPDDR4x internal setting value by VREF Training.

8.2.3 Single-Ended Input Voltage for Clock

The minimum input voltage need to satisfy both V_{inse_CK} , $V_{inse_CK_High/Low}$ specification at input receiver.

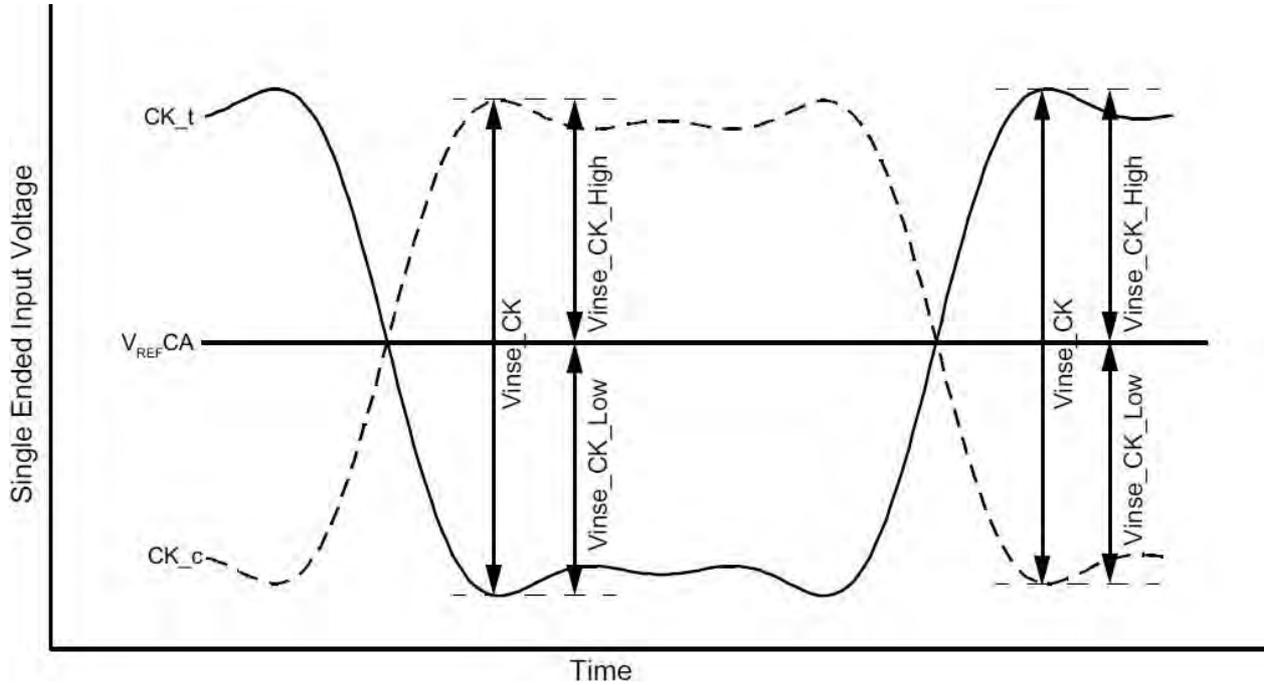


Figure 9. Clock Single-Ended Input Voltage

NOTE:

1) VREFCA is LPDDR4x internal setting value by VREF Training.

[Table 30] Clock Single-Ended input voltage

| Parameter | Symbol | Data Rate | | | | | | Unit |
|---|----------------------|-------------------------|-----|----------------|-----|-----------|-----|------|
| | | 1600/1866 ¹⁾ | | 2133/2400/3200 | | 3733/4266 | | |
| | | Min | Max | Min | Max | Min | Max | |
| Clock Single-Ended input voltage | V_{inse_CK} | 210 | - | 190 | - | 180 | - | mV |
| Clock Single-Ended input voltage High from VREFDQ | $V_{inse_CK_High}$ | 105 | - | 95 | - | 90 | - | mV |
| Clock Single-Ended input voltage Low from VREFDQ | $V_{inse_CK_Low}$ | 105 | - | 95 | - | 90 | - | mV |

NOTE :

1) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.2.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 10. and the following Tables.

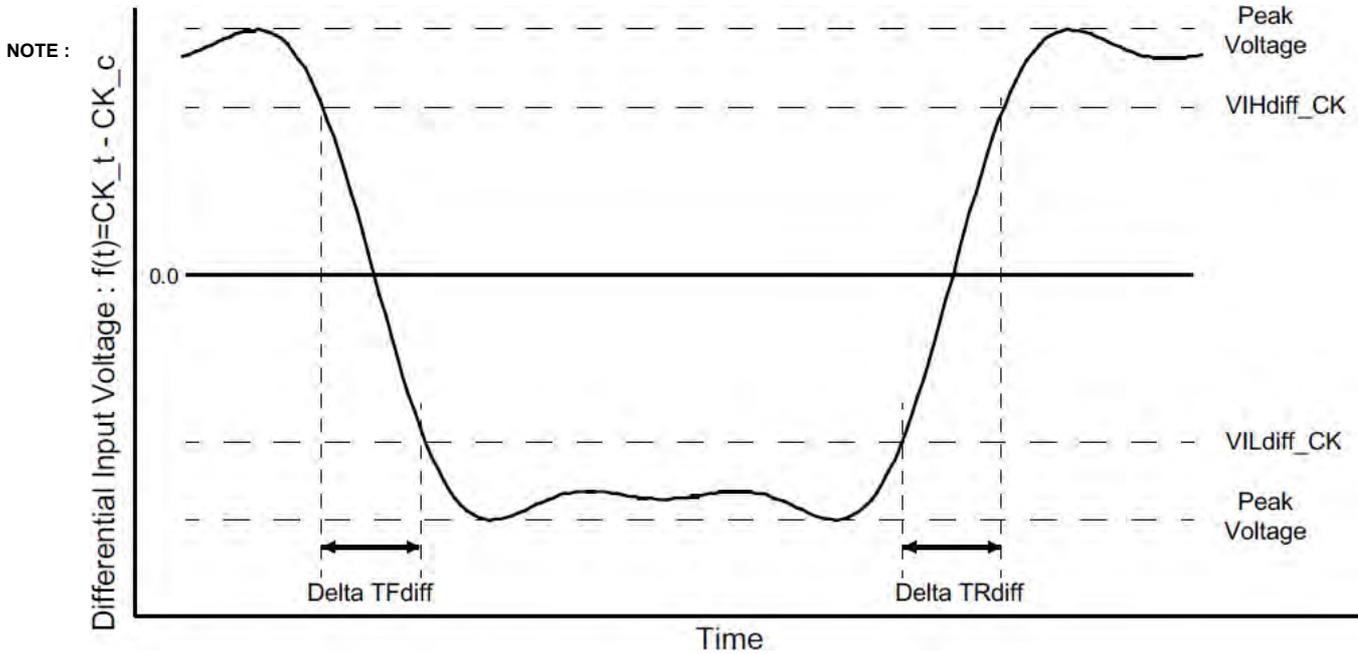


Figure 10. Differential Input Slew Rate Definition for CK_t, CK_c

- 1) Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
- 2) Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

[Table 31] Differential Input Slew Rate Definition for CK_t, CK_c

| Description | From | To | Defined by |
|---|------------|------------|---|
| Differential input slew rate for rising edge(CK _t - CK _c) | VILdiff_CK | VIHdiff_CK | $ VILdiff_CK - VIHdiff_CK /DeltaTRdiff$ |
| Differential input slew rate for falling edge(CK _t - CK _c) | VIHdiff_CK | VILdiff_CK | $ VILdiff_CK - VIHdiff_CK /DeltaTFdiff$ |

[Table 32] Differential Input Level for CK_t, CK_c

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|-------------------------|------------|-------------------------|------|----------------|------|-----------|------|------|------|
| | | 1600/1866 ¹⁾ | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input High | VIHdiff_CK | 175 | - | 155 | - | 145 | - | mV | |
| Differential Input Low | VILdiff_CK | - | -175 | - | -155 | - | -145 | mV | |

NOTE :

- 1) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

[Table 33] Differential Input Slew Rate for CK_t, CK_c

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|--|-------------|-----------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input Slew Rate for Clock | SRIldiff_CK | 2 | 14 | 2 | 14 | 2 | 14 | V/ns | |

8.2.5 Differential Input Cross Point Voltage for Clock

The cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in [Table 34]. The differential input cross point voltage V_{IX} is measured from the actual cross point of true and complement signals to the mid level that is V_{REFCA}.

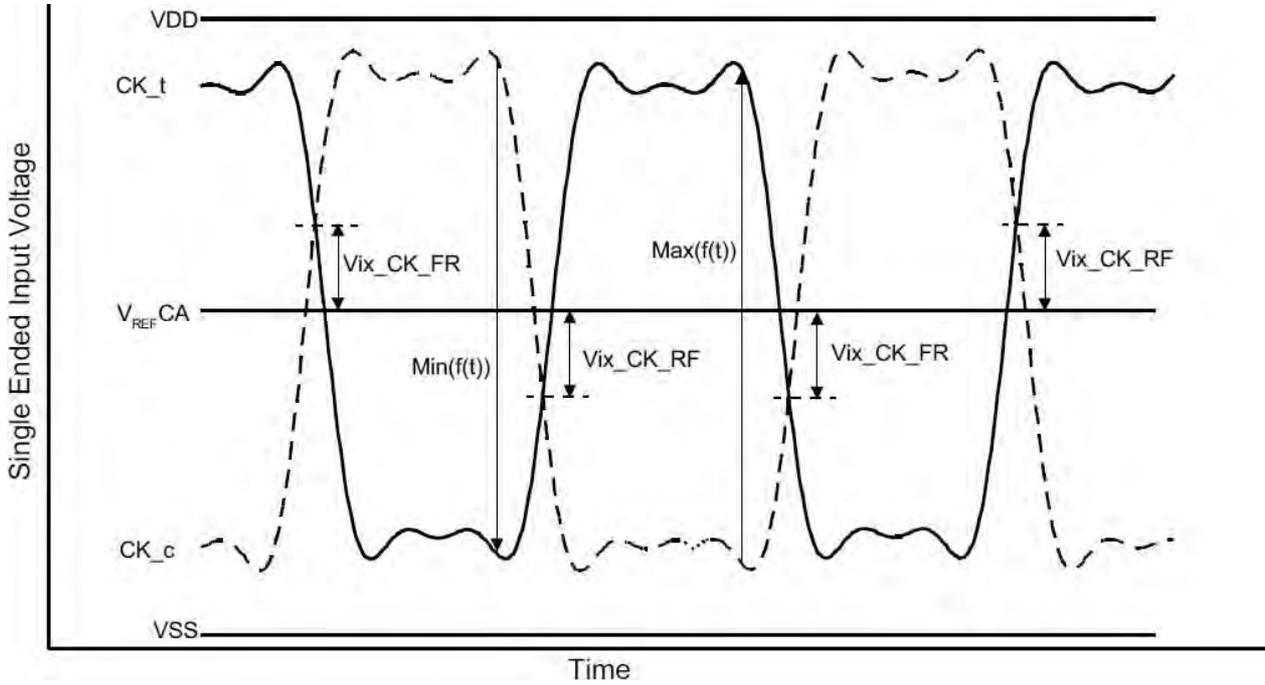


Figure 11. Vix Definition (Clock)

[Table 34] Cross point voltage for differential input signals (Clock)

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|--|--------------|-------------------------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 ^{a)} | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Clock Differential input cross point voltage ratio | Vix_CK_ratio | - | 25 | - | 25 | - | 25 | % | 1,2 |

NOTE :

1) Vix_CK_Ratio is defined by this equation: $Vix_CK_Ratio = Vix_CK_FR / |Min(f(t))|$

2) Vix_CK_Ratio is defined by this equation: $Vix_CK_Ratio = Vix_CK_RF / Max(f(t))$

a) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.2.6 AC/DC Input level for ODT input

[Table 35] LPDDR4x Input Level for ODT

| Symbol | | Min | Max | Unit | Note |
|-----------------|---------------------------|----------------------|----------------------|------|------|
| $V_{IHODT(AC)}$ | ODT Input High Level (AC) | $0.75 \times V_{DD}$ | $V_{DD} + 0.2$ | V | 1 |
| $V_{ILODT(AC)}$ | ODT Input Low Level (AC) | -0.2 | $0.25 \times V_{DD}$ | V | 1 |
| $V_{IHODT(DC)}$ | ODT Input High Level (DC) | $0.65 \times V_{DD}$ | $V_{DD} + 0.2$ | V | |
| $V_{ILODT(DC)}$ | ODT Input Low Level (DC) | -0.2 | $0.35 \times V_{DD}$ | V | |

NOTE :

1) See Overshoot and Undershoot Specifications.

8.2.7 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both V_{indiff_DQS} and $V_{indiff_DQS} / 2$ specification at input receiver and their measurement period is $1UI(t_{CK} / 2)$.
 2) V_{indiff_DQS} is the peak to peak voltage centered on 0 volts differential and $V_{indiff_DQS} / 2$ is max and min peak voltage from 0V.

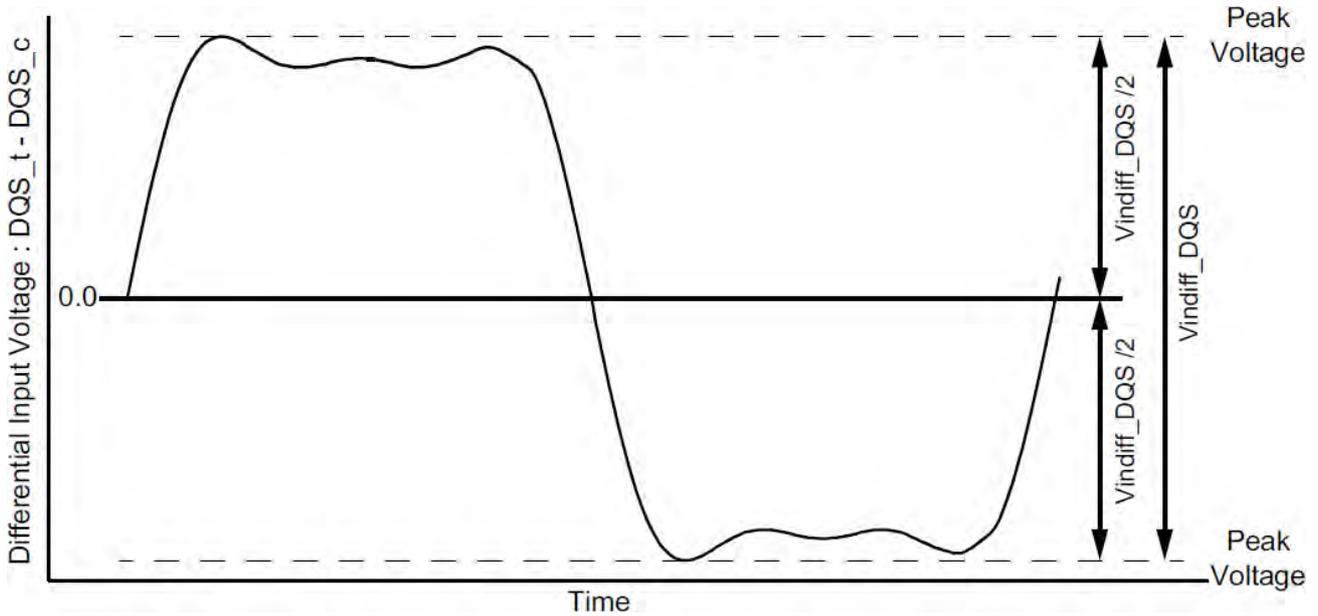


Figure 12. DQS Differential Input Voltage

[Table 36] DQS differential input voltage

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|------------------------|-------------------|-------------------------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 ^{a)} | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS differential input | V_{indiff_DQS} | 360 | - | 360 | - | 340 | - | mV | 1 |

NOTE :

1) The peak voltage of Differential DQS signals is calculated in a following equation.

$$V_{indiff_DQS} = (\text{Max Peak Voltage}) - (\text{Min Peak Voltage})$$

$$\text{Max Peak Voltage} = \text{Max}(f(t))$$

$$\text{Min Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = VDQS_t - VDQS_c$$

a) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.2.8 Peak voltage calculation method

The peak voltage of Differential DQS signals are calculated in a following equation.

$$\text{VIH.DIFF.Peak Voltage} = \text{Max}(f(t))$$

$$\text{VIL.DIFF.Peak Voltage} = \text{Min}(f(t))$$

$$f(t) = \text{VDQS}_t - \text{VDQS}_c$$

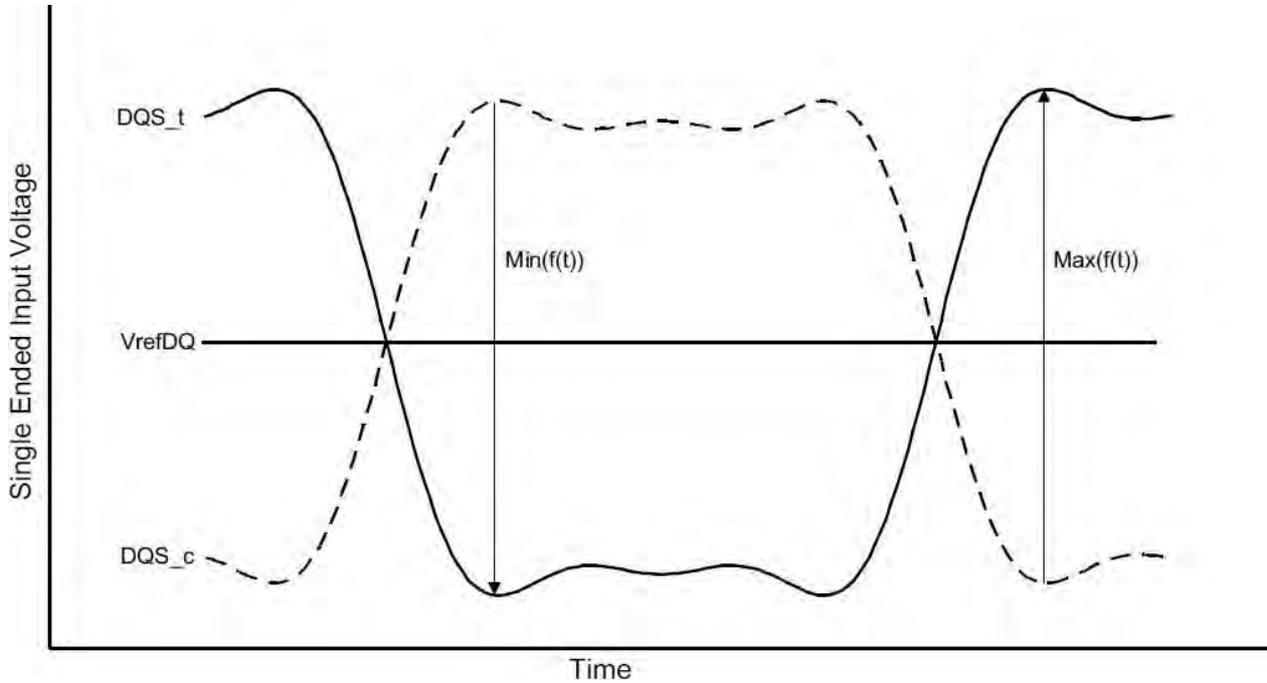


Figure 13. Definition of differential DQS Peak Voltage

8.2.9 Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both V_{inse_DQS} , $V_{inse_DQS_High/Low}$ specification at input receiver.

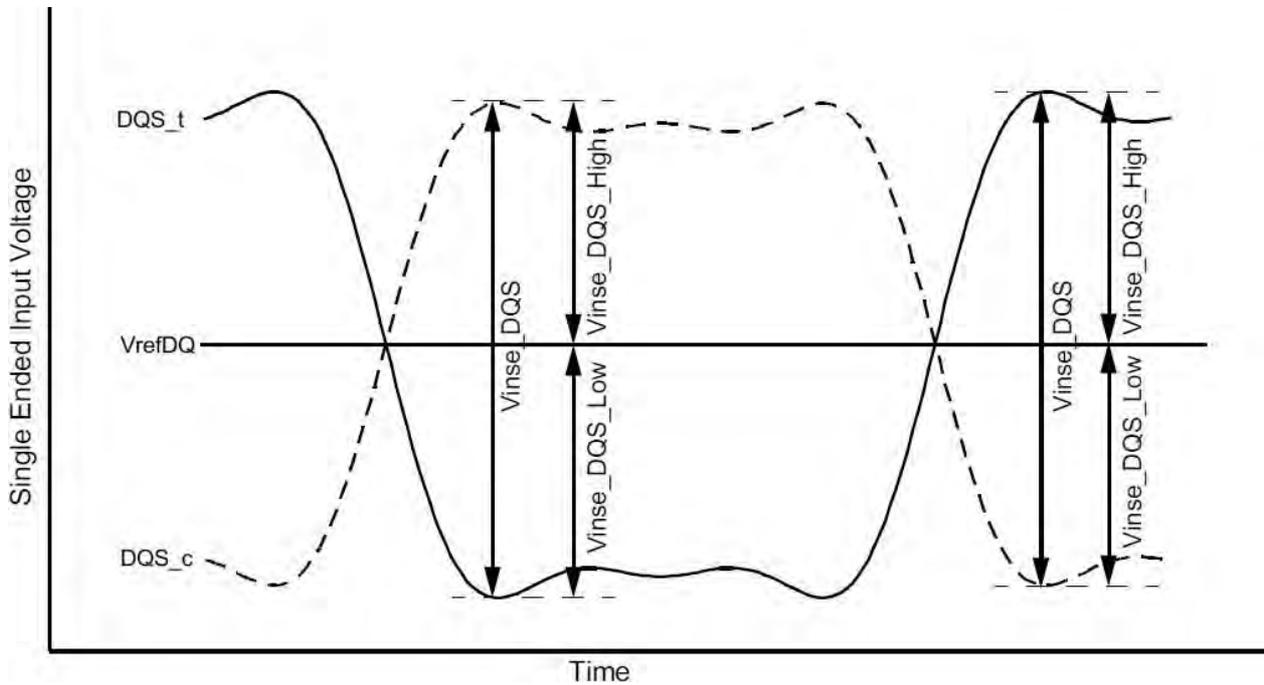


Figure 14. DQS Single-Ended Input Voltage

[Table 37] DQS Single-Ended input voltage

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|---|-----------------------|-------------------------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 ^{a)} | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS Single-Ended input voltage | V_{inse_DQS} | 180 | - | 180 | - | 170 | - | mV | |
| DQS Single-Ended input voltage High from VrefDQ | $V_{inse_DQS_High}$ | 90 | - | 90 | - | 85 | - | mV | |
| DQS Single-Ended input voltage Low from VrefDQ | $V_{inse_DQS_Low}$ | 90 | - | 90 | - | 85 | - | mV | |

NOTE :

1) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.2.10 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 15. and [Table 38].

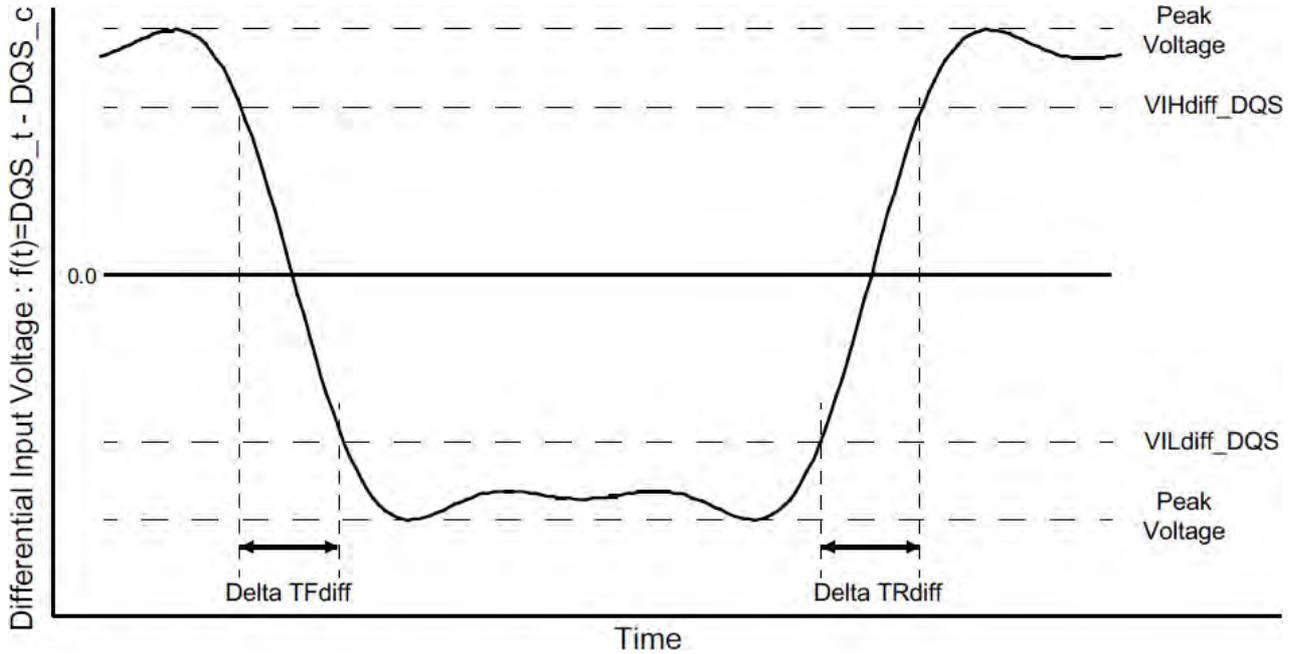


Figure 15. Differential Input Slew Rate Definition for DQS_t, DQS_c

[Table 38] Differential Input Slew Rate Definition for DQS_t, DQS_c

| Description | From | To | Defined by |
|--|-------------|-------------|---|
| Differential input slew rate for rising edge (DQS _t - DQS _c) | VILdiff_DQS | VIHdiff_DQS | $ VILdiff_DQS - VIHdiff_DQS / \Delta TRdiff$ |
| Differential input slew rate for falling edge (DQS _t - DQS _c) | VIHdiff_DQS | VILdiff_DQS | $ VILdiff_DQS - VIHdiff_DQS / \Delta TFdiff$ |

[Table 39] Differential Input Level for DQS_t, DQS_c

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|-------------------------|-------------|-------------------------|------|----------------|------|-----------|------|------|------|
| | | 1600/1866 ¹⁾ | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input High | VIHdiff_DQS | 140 | - | 140 | - | 120 | - | mV | |
| Differential Input Low | VILdiff_DQS | - | -140 | - | -140 | - | -120 | mV | |

NOTE :

1) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

[Table 40] Differential Input Slew Rate for DQS_t, DQS_c

| Parameter | Symbol | Data Rate | | | | | | Unit | Note |
|------------------------------|---------|-----------|-----|----------------|-----|-----------|-----|------|------|
| | | 1600/1866 | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| Differential Input Slew Rate | SRIdiff | 2 | 14 | 2 | 14 | 2 | 14 | V/ns | |

8.3 Differential Input Cross Point Voltage for DQS

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in [Table 41]. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is V_{REFDQ}.

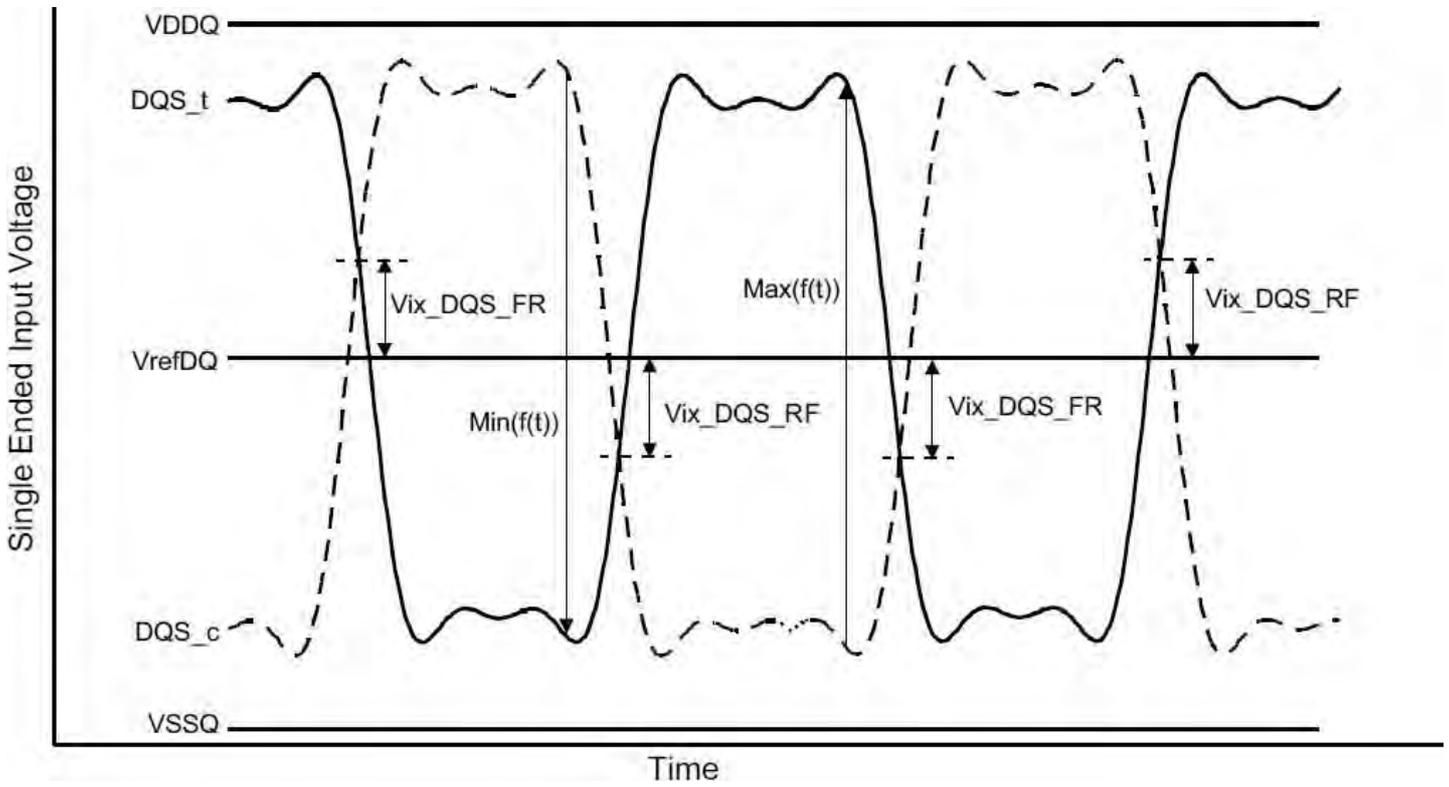


Figure 16. Vix Definition (DQS)

[Table 41] Cross point voltage for differential input signals (DQS)

| Parameter | Symbol | Data Rate | | | | | | Units | Notes |
|---|---------------|-------------------------|-----|----------------|-----|-----------|-----|-------|-------|
| | | 1600/1866 ³⁾ | | 2133/2400/3200 | | 3733/4266 | | | |
| | | Min | Max | Min | Max | Min | Max | | |
| DQS Differential input crosspoint voltage ratio | Vix_DQS_ratio | - | 20 | - | 20 | - | 20 | % | 1,2 |

NOTE :

1) Vix_DQS_Ratio is defined by this equation: $Vix_DQS_Ratio = Vix_DQS_FR / |Min(f(t))|$

2) Vix_DQS_Ratio is defined by this equation: $Vix_DQS_Ratio = Vix_DQS_RF / Max(f(t))$

3) The following requirements apply for DQ operating frequencies at or below 1333Gbps for all speed bins for the first column 1600/1866.

8.4 Single Ended Output Slew Rate

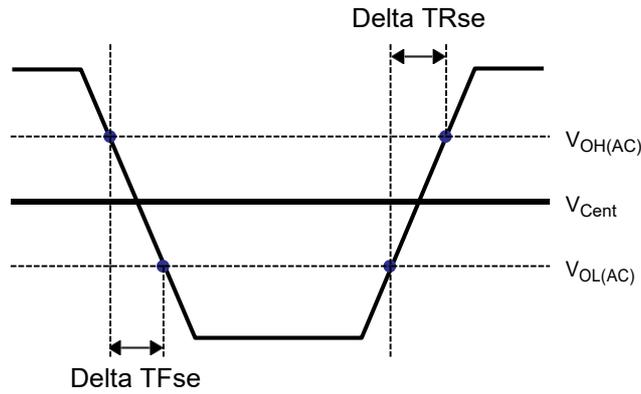


Figure 17. Single Ended Output Slew Rate Definition

[Table 42] Output Slew Rate (single-ended) for 0.6V VDDQ

| Parameter | Symbol | Value | | Units |
|--|------------|-------------------|-------------------|-------|
| | | Min ¹⁾ | Max ²⁾ | |
| Single-ended Output Slew Rate ($V_{OH} = V_{DDQ} \times 0.5$) | S_{RQse} | 3.0 | 9.0 | V/ns |
| Output slew-rate matching Ratio (Rise to Fall) | | 0.8 | 1.2 | - |
| Description: | | | | |
| SR: Slew Rate | | | | |
| Q: Query Output (like in DQ, which stands for Data-in, Query-Output) | | | | |
| se: Single-ended Signals | | | | |

- NOTE :**
- 1) Measured with output reference load.
 - 2) The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
 - 3) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = 0.2 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
 - 4) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.5 Differential Output Slew Rate

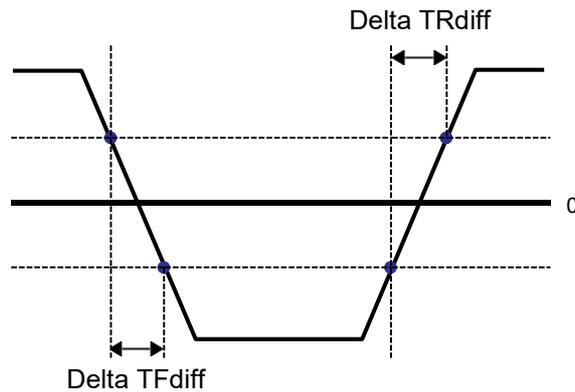


Figure 18. Differential Output Slew Rate Definition

[Table 43] Differential Output Slew Rate for 0.6V VDDQ

| Parameter | Symbol | Value | | Units |
|---|---------|-------|------|-------|
| | | Min | Max | |
| Differential Output Slew Rate ($V_{OH} = VDDQ \times 0.5$) | SRQdiff | 6 | 18.0 | V/ns |
| Description: SR: Slew Rate Q: Query Output (like in DQ, which stands for Data-in, Query-Output) diff: Differential Signals | | | | |

NOTE :

- 1) Measured with output reference load.
- 2) The output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)} = -0.8 \times V_{OH(DC)}$ and $V_{OH(AC)} = 0.8 \times V_{OH(DC)}$.
- 3) Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

8.6 Overshoot and Undershoot for LVSTL

[Table 44] AC Overshoot/Undershoot Specification

| Parameter | | Data Rate | | | | | Units |
|--|-----|-----------|------|------------|------|------|-------|
| | | 1600 | 1866 | 3200 | 3733 | 4266 | |
| Maximum peak amplitude allowed for overshoot area. (See Figure 6.) | Max | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V |
| Maximum peak amplitude allowed for undershoot area. (See Figure 6.) | Max | 0.3 | 0.3 | 0.3 | 0.3 | 0.3 | V |
| Maximum overshoot area above V_{DD} . (See Figure 6.) | Max | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V-ns |
| Maximum undershoot area below V_{SS} . (See Figure 6.) | Max | 0.1 | 0.1 | 0.1 | 0.1 | 0.1 | V-ns |

NOTE :

- 1) V_{DD2} stands for V_{DD} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{DD} stands for V_{DDQ} for DQ, DMI, DQS_t and DQS_c.
- 2) V_{SS} stands for V_{SS} for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. V_{SS} stands for V_{SSQ} for DQ, DMI, DQS_t and DQS_c.
- 3) Maximum peak amplitude values are referenced from actual V_{DD} and V_{SS} values.
- 4) Maximum area values are referenced from maximum operating V_{DD} and V_{SS} values.

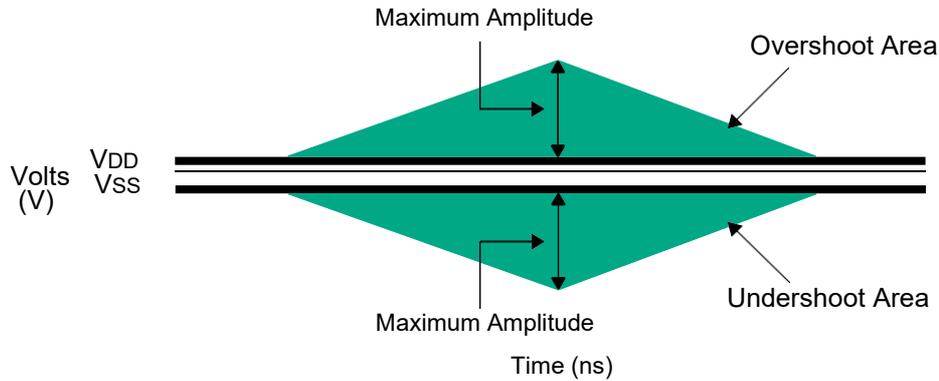


Figure 19. Overshoot and Undershoot Definition

9 OUTPUT BUFFER CHARACTERISTICS

9.0 LPDDR4x Driver Output Timing Reference Load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

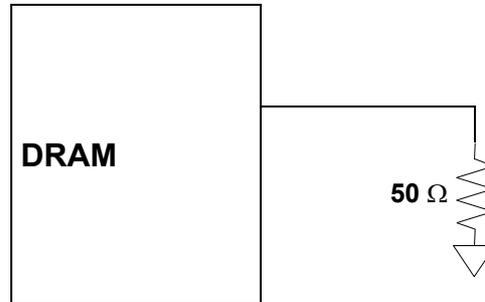


Figure 20. Driver Output Reference Load for Timing and Slew Rate

NOTE :

1) All output timing parameter values are reported with respect to this reference load. This reference load is also used to report slew rate.

9.1 LVSTL (Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down driver and a terminator. The basic cell is shown in Figure 21 .

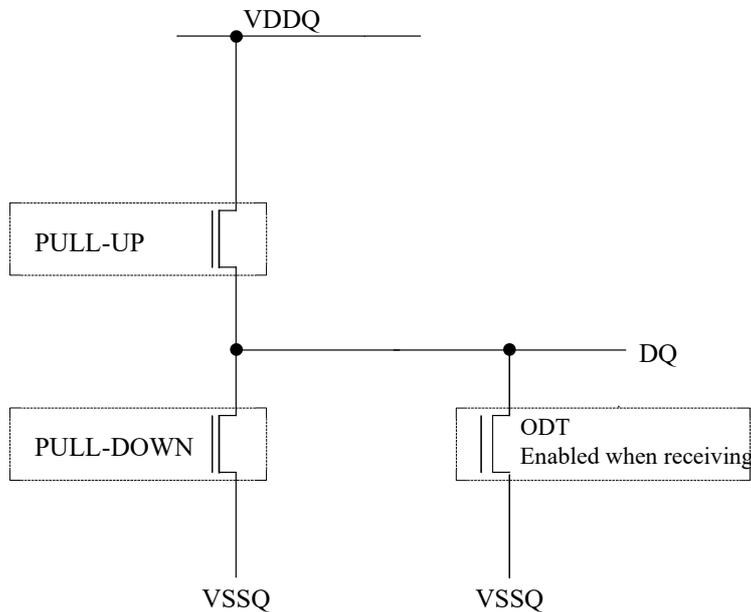


Figure 21. LVSTL I/O Cell

To ensure that the target impedance is achieved the LVSTL I/O cell is designed to calibrated as below procedure.

- 1) First calibrate the pull-down device against a 240 Ohm resistor to VDDQ via the ZQ pin
 - Set Strength Control to minimum setting
 - Increase drive strength until comparator detects data bit is less than VDDQ/2.
 - NMOS pull-down device is calibrated to 240 Ohms

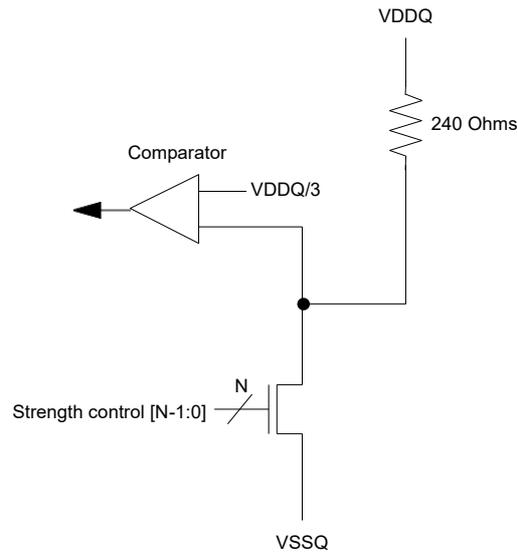


Figure 22. pull-down calibration

2) Then calibrate the pull-up device against the calibrated pull-down device.

Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS)

Set Strength Control to minimum setting

Increase drive strength until comparator detects data bit is greater than VOH target

NMOS pull-up device is now calibrated to VOH target

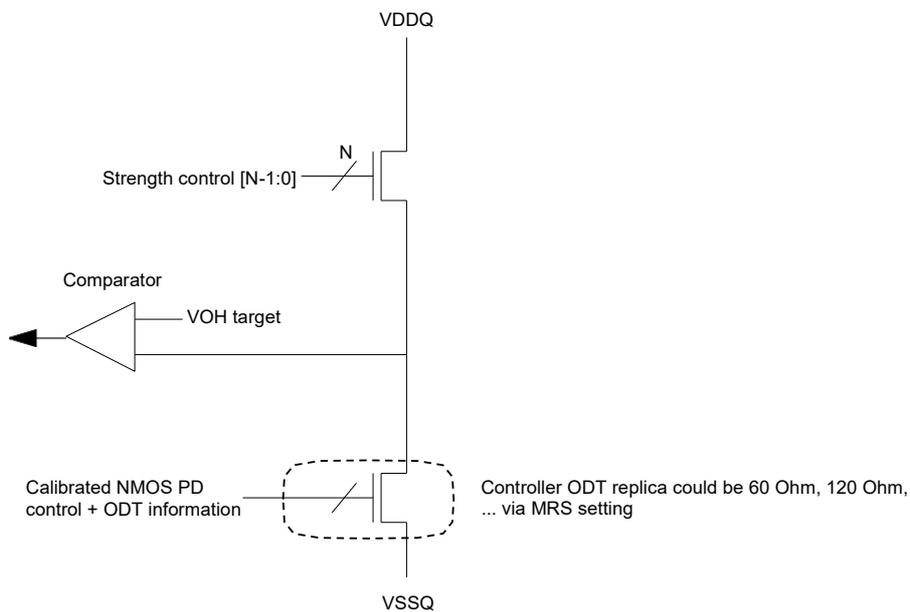


Figure 23. pull-up calibration

10. INPUT/OUTPUT CAPACITANCE

[Table 45] Input/Output Capacitance

| Parameter | Symbol | Min/Max | Value | Unit | Notes |
|--|--------|---------|-------|------|-------|
| Input capacitance, CK_t and CK_c | CCK | Min | 0.5 | pF | 1,2 |
| | | Max | 0.9 | | |
| Input capacitance delta, CK_t and CK_c | CDCK | Min | 0.0 | pF | 1,2,3 |
| | | Max | 0.09 | | |
| Input capacitance, all other input-only pins | CI | Min | 0.5 | pF | 1,2,4 |
| | | Max | 0.9 | | |
| Input capacitance delta, all other input-only pins | CDI | Min | -0.1 | pF | 1,2,5 |
| | | Max | 0.1 | | |
| Input/output capacitance, DQ, DMI, DQS_t and DQS_c | CIO | Min | 0.7 | pF | 1,2,6 |
| | | Max | 1.3 | | |
| Input/output capacitance delta, DQS_t and DQS_c | CDDQS | Min | 0.0 | pF | 1,2,7 |
| | | Max | 0.1 | | |
| Input/output capacitance delta, DQ and DMI | CDIO | Min | -0.1 | pF | 1,2,8 |
| | | Max | 0.1 | | |
| Input/output capacitance ZQ pin | CZQ | Min | 0.0 | pF | 1,2 |
| | | Max | 0.5 | | |

NOTE :

- 1) This parameter applies to both die and package.
- 2) This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with VDD1, VDD2, VDDQ, VSS, VSSQ applied and all other pins floating).
- 3) Absolute value of CCK_t - CCK_c.
- 4) CI applies to CS_n, CKE, CA0-CA5.
- 5) $CDI = CI - 0.5 \times (CCK_t + CCK_c)$
- 6) DMI loading matches DQ and DQS.
- 7) Absolute value of CDQS_t and CDQS_c.
- 8) $CDIO = CIO - 0.5 \times (CDQS_t + CDQS_c)$ in byte-lane.

11 IDD SPECIFICATION PARAMETERS AND TEST CONDITIONS

11.0 IDD Measurement Conditions

The following definitions are used within the IDD measurement tables unless stated otherwise:

LOW: $V_{IN} \leq V_{IL}(DC) \text{ MAX}$

HIGH: $V_{IN} \geq V_{IH}(DC) \text{ MIN}$

STABLE: Inputs are stable at a HIGH or LOW level

SWITCHING: See Table 46 and Table 47.

[Table 46] Definition of Switching for CA Input Signals

| Switching for CA | | | | | | | | |
|------------------|------|------|------|------|------|------|------|------|
| CK_t edge | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 |
| CKE | HIGH |
| CS | LOW |
| CA0 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA1 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA2 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA3 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |
| CA4 | HIGH | LOW | LOW | LOW | LOW | HIGH | HIGH | HIGH |
| CA5 | HIGH | HIGH | HIGH | LOW | LOW | LOW | LOW | HIGH |

NOTE :

1) CS must always be driven LOW.

2) 50% of CA bus is changing between HIGH and LOW once per clock for the CA bus.

3) The above pattern is used continuously during IDD measurement for IDD values that require switching on the CA bus.

[Table 47] CA pattern for IDD4R for BL=16

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Read-1 | L | H | L | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | H | H | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

NOTE :

1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B, Burst Order CA[3:2] = 00_B or 11_B (Same as LPDDR3 IDD4R Spec)

2) Difference from LPDDR3 Spec : CA pins are kept low with DES CMD to reduce ODT current.

[Table 48] CA pattern for IDD4W for BL=16

| Clock Cycle Number | CKE | CS | Command | CA0 | CA1 | CA2 | CA3 | CA4 | CA5 |
|--------------------|------|------|---------|-----|-----|-----|-----|-----|-----|
| N | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+1 | HIGH | LOW | | L | H | L | L | L | L |
| N+2 | HIGH | HIGH | CAS-2 | L | H | L | L | H | L |
| N+3 | HIGH | LOW | | L | L | L | L | L | L |
| N+4 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+5 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+6 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+7 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+8 | HIGH | HIGH | Write-1 | L | L | H | L | L | L |
| N+9 | HIGH | LOW | | L | H | L | L | H | L |
| N+10 | HIGH | HIGH | CAS-2 | L | H | L | L | H | H |
| N+11 | HIGH | LOW | | L | L | H | H | H | H |
| N+12 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+13 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+14 | HIGH | LOW | DES | L | L | L | L | L | L |
| N+15 | HIGH | LOW | DES | L | L | L | L | L | L |

NOTE :

 1) BA[2:0] = 010_B, CA[9:4] = 000000_B or 111111_B (.

[Table 49] Data Pattern for IDD4W (DBI off) for BL=16

| DBI OFF Case | | | | | | | | | | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

NOTE:

1) Simplified pattern compared with last showing.

Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 50] Data Pattern for IDD4R (DBI off) for BL=16

| DBI OFF Case | | | | | | | | | | No. of 1's |
|--------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 8 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 6 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | | |

NOTE:
1) Same data pattern was applied to DQ[4], DQ[5], DQ[6], DQ[7] for reducing complexity for IDD4W/R pattern programming.

[Table 51] Data Pattern for IDD4W (DBI on) for BL=16

| DBI ON Case | | | | | | | | | | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| | | | | | | | | | | |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL21 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL23 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL29 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL31 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| No. of 1's | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

 DBI enabled burst

[Table 52] Data Pattern for IDD4R (DBI on) for BL=16

| DBI ON Case | | | | | | | | | | No. of 1's |
|-------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|------------|
| | DQ[7] | DQ[6] | DQ[5] | DQ[4] | DQ[3] | DQ[2] | DQ[1] | DQ[0] | DBI | |
| BL0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL3 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL5 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL7 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL8 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL9 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL10 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL11 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL12 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL13 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL15 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL16 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL17 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL18 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL19 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL20 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL21 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL22 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL23 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL24 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| BL25 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL26 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| BL27 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| BL28 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 2 |
| BL29 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 4 |
| BL30 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 3 |
| BL31 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 4 |
| No. of 1's | 8 | 8 | 8 | 8 | 8 | 8 | 16 | 16 | 8 | |

11.1 IDD Specifications

IDD values are for the entire operating voltage range, and all of them are for the entire standard range, with the exception of IDD6ET which is for the entire elevated temperature range.

[Table 53] LPDDR4x IDD Specification Parameters and Operating Conditions

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|---------------------|--------------|-----------|
| Operating one bank active-precharge current: $t_{CK} = t_{CKmin}$; $t_{RC} = t_{RCmin}$; CE is HIGH; CS is LOW between valid commands; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD0 ₁ | VDD1 | 1,10,11 |
| | IDD0 ₂ | VDD2 | 1,10,11 |
| | IDD0 _Q | VDDQ | 1,3,10,11 |
| Idle power-down standby current: $t_{CK} = t_{CKmin}$; CE is LOW; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2P ₁ | VDD1 | 1,10,11 |
| | IDD2P ₂ | VDD2 | 1,10,11 |
| | IDD2P _Q | VDDQ | 1,3,10,11 |
| Idle power-down standby current with clock stop: CK _t =LOW, CK _c =HIGH; CE is LOW; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2PS ₁ | VDD1 | 1,10,11 |
| | IDD2PS ₂ | VDD2 | 1,10,11 |
| | IDD2PS _Q | VDDQ | 1,3,10,11 |
| Idle non power-down standby current: $t_{CK} = t_{CKmin}$; CE is HIGH; CS is LOW; All banks are idle; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD2N ₁ | VDD1 | 1,10,11 |
| | IDD2N ₂ | VDD2 | 1,10,11 |
| | IDD2N _Q | VDDQ | 1,3,10,11 |
| Idle non power-down standby current with clock stopped: CK _t =LOW; CK _c =HIGH; CE is HIGH; CS is LOW; All banks are idle; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD2NS ₁ | VDD1 | 1,10,11 |
| | IDD2NS ₂ | VDD2 | 1,10,11 |
| | IDD2NS _Q | VDDQ | 1,3,10,11 |
| Active power-down standby current: $t_{CK} = t_{CKmin}$; CE is LOW; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD3P ₁ | VDD1 | 1,10,11 |
| | IDD3P ₂ | VDD2 | 1,10,11 |
| | IDD3P _Q | VDDQ | 1,3,10,11 |
| Active power-down standby current with clock stop: CK _t =LOW, CK _c =HIGH; CE is LOW; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD3PS ₁ | VDD1 | 1,10,11 |
| | IDD3PS ₂ | VDD2 | 1,10,11 |
| | IDD3PS _Q | VDDQ | 1,4,10,11 |

[Table 53] LPDDR4x IDD Specification Parameters and Operating Conditions

| Parameter/Condition | Symbol | Power Supply | Notes |
|---|---------------------|--------------|---------------|
| Active non-power-down standby current: $t_{CK} = t_{CKmin}$; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are switching; Data bus inputs are stable ODT disabled | IDD3N ₁ | VDD1 | 1,10,11 |
| | IDD3N ₂ | VDD2 | 1,10,11 |
| | IDD3N _Q | VDDQ | 1,4,10,11 |
| Active non-power-down standby current with clock stopped: CK _t =LOW, CK _c =HIGH; CKE is HIGH; CS is LOW; One bank is active; CA bus inputs are stable; Data bus inputs are stable ODT disabled | IDD3NS ₁ | VDD1 | 1,10,11 |
| | IDD3NS ₂ | VDD2 | 1,10,11 |
| | IDD3NS _Q | VDDQ | 1,4,10,11 |
| Operating burst READ current: $t_{CK} = t_{CKmin}$; CS is LOW between valid commands; One bank is active; BL = 16 or 32; RL = RL(MIN); CA bus inputs are switching; 50% data change each burst transfer ODT disabled | IDD4R ₁ | VDD1 | 1,10,11 |
| | IDD4R ₂ | VDD2 | 1,10,11 |
| | IDD4R _Q | VDDQ | 1,5,10,11 |
| Operating burst WRITE current: $t_{CK} = t_{CKmin}$; CS is LOW between valid commands; One bank is active; BL = 16 or 32; WL = WLmin; CA bus inputs are switching; 50% data change each burst transfer ODT disabled | IDD4W ₁ | VDD1 | 1,10,11 |
| | IDD4W ₂ | VDD2 | 1,10,11 |
| | IDD4W _Q | VDDQ | 1,4,10,11 |
| All-bank REFRESH Burst current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{RFCabmin}$; Burst refresh; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5 ₁ | VDD1 | 1,10,11 |
| | IDD5 ₂ | VDD2 | 1,10,11 |
| | IDD5 _Q | VDDQ | 1,4,10,11 |
| All-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5AB ₁ | VDD1 | 1,10,11 |
| | IDD5AB ₂ | VDD2 | 1,10,11 |
| | IDD5AB _Q | VDDQ | 1,4,10,11 |
| Per-bank REFRESH Average current: $t_{CK} = t_{CKmin}$; CKE is HIGH between valid commands; $t_{RC} = t_{REFI}/8$; CA bus inputs are switching; Data bus inputs are stable; ODT disabled | IDD5PB ₁ | VDD1 | 1,10,11 |
| | IDD5PB ₂ | VDD2 | 1,10,11 |
| | IDD5PB _Q | VDDQ | 1,4,10,11 |
| Power Down Self refresh current (-40°C to +95°C): CK _t =LOW, CK _c =HIGH; CKE is LOW; CA bus inputs are stable; Data bus inputs are stable; Maximum 1x Self-Refresh Rate; ODT disabled | IDD6 ₁ | VDD1 | 6,7,9,10,11 |
| | IDD6 ₂ | VDD2 | 6,7,9,10,11 |
| | IDD6 _Q | VDDQ | 4,6,7,9,10,11 |

NOTE=

- 1) Published IDD values are the maximum of the distribution of the arithmetic mean.
- 2) ODT disabled: MR11[2:0] = 000_B.
- 3) IDD current specifications are tested after the device is properly initialized.
- 4) Measured currents are the summation of VDDQ and VDD2.
- 5) Guaranteed by design with output load = 5pF and RON = 40 ohm.
- 6) The 1x Self-Refresh Rate is the rate at which the LPDDR4x device is refreshed internally during Self-Refresh, before going into the elevated Temperature range.
- 7) This is the general definition that applies to full array Self Refresh.
- 8) For all IDD measurements, VIHCKE = 0.8 x VDD2, VILCKE = 0.2 x VDD2.
- 9) IDD6 25°C is guaranteed, IDD6 95°C is typical of the distribution of the arithmetic mean.
- 10) These specification values are the summation of all the channel current and both channels are under the same condition at the same time.
- 11) Dual Channel devices are specified in dual channel operation (both channels operating together).

11.2 IDD Spec Table

[Table 54] IDD Specification (Temp: -40°C ~ 95°C)

a. For 8Gb and 16Gb

| Symbol | | Power Supply | 8Gb 1ch x16 | 16Gb 2ch x32 | 16Gb 2ch x32 | Units |
|--------|---------------------|--------------|-------------|--------------|--------------|-------|
| | | | 3733Mbps | 3733Mbps | 4266Mbps | |
| IDD0 | IDD0 ₁ | VDD1 | 5 | 10 | 10 | mA |
| | IDD0 ₂ | VDD2 | 32.5 | 65 | 65 | mA |
| | IDD0 _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD2P | IDD2P ₁ | VDD1 | 1 | 2 | 2 | mA |
| | IDD2P ₂ | VDD2 | 3.13 | 6.26 | 6.26 | mA |
| | IDD2P _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD2PS | IDD2PS ₁ | VDD1 | 1 | 2 | 2 | mA |
| | IDD2PS ₂ | VDD2 | 3.13 | 6.26 | 6.26 | mA |
| | IDD2PS _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD2N | IDD2N ₁ | VDD1 | 1.5 | 3 | 3 | mA |
| | IDD2N ₂ | VDD2 | 13.25 | 26.5 | 26.5 | mA |
| | IDD2N _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD2NS | IDD2NS ₁ | VDD1 | 1.5 | 3 | 3 | mA |
| | IDD2NS ₂ | VDD2 | 9.31 | 18.62 | 20.5 | mA |
| | IDD2NS _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD3P | IDD3P ₁ | VDD1 | 1.4 | 2.8 | 2.8 | mA |
| | IDD3P ₂ | VDD2 | 6.75 | 13.5 | 13.5 | mA |
| | IDD3P _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD3PS | IDD3PS ₁ | VDD1 | 1.4 | 2.8 | 2.8 | mA |
| | IDD3PS ₂ | VDD2 | 6.75 | 13.5 | 13.5 | mA |
| | IDD3PS _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD3N | IDD3N ₁ | VDD1 | 1.5 | 3 | 3 | mA |
| | IDD3N ₂ | VDD2 | 16 | 31.7 | 34 | mA |
| | IDD3N _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD3NS | IDD3NS ₁ | VDD1 | 1.5 | 3 | 3 | mA |
| | IDD3NS ₂ | VDD2 | 14 | 28 | 30 | mA |
| | IDD3NS _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD4R | IDD4R ₁ | VDD1 | 20.6 | 41.2 | 46 | mA |
| | IDD4R ₂ | VDD2 | 207.7 | 415.4 | 465 | mA |
| | IDD4R _Q | VDDQ | 88.1 | 176.2 | 185 | mA |
| IDD4W | IDD4W ₁ | VDD1 | 20.5 | 41 | 41 | mA |
| | IDD4W ₂ | VDD2 | 208.1 | 416.2 | 460 | mA |
| | IDD4W _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD5 | IDD5 ₁ | VDD1 | 34.7 | 69.4 | 75 | mA |
| | IDD5 ₂ | VDD2 | 136.3 | 273 | 300 | mA |
| | IDD5 _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD5AB | IDD5AB ₁ | VDD1 | 3.5 | 7 | 7 | mA |
| | | VDD2 | 18 | 36 | 40 | mA |
| | | VDDQ | 0.25 | 0.5 | 0.5 | mA |

| Symbol | | Power Supply | 8Gb 1ch x16 | 16Gb 2ch x32 | 16Gb 2ch x32 | Units |
|--------|---------------------|--------------|-------------|--------------|--------------|-------|
| | | | 3733Mbps | 3733Mbps | 4266Mbps | |
| IDD5PB | IDD5PB ₁ | VDD1 | 3.5 | 7 | 7 | mA |
| | IDD5PB ₂ | VDD2 | 18.5 | 37 | 41 | mA |
| | IDD5PB _Q | VDDQ | 0.25 | 0.5 | 0.5 | mA |
| IDD6 | IDD6 ₁ | 25°C | VDD1 | 0.5 | 1 | mA |
| | | 95°C | | 2.5 | 10 | |
| | IDD6 ₂ | 25°C | VDD2 | 1.35 | 2.7 | mA |
| | | 95°C | | 11 | 44 | |
| | IDD6 _Q | 25°C | VDDQ | 0.2 | 0.4 | mA |
| | | 95°C | | 0.25 | 0.5 | mA |

NOTE :

1) These specification values are measured on single chip condition.

b. For 32Gb

| Symbol | | Power Supply | 32Gb 2ch x32 | | |
|--------|---------------------|--------------|--------------|----------|-------|
| | | | 3733Mbps | 4266Mbps | Units |
| IDD0 | IDD0 ₁ | VDD1 | TBD | TBD | mA |
| | IDD0 ₂ | VDD2 | TBD | TBD | mA |
| | IDD0 _Q | VDDQ | TBD | TBD | mA |
| IDD2P | IDD2P ₁ | VDD1 | TBD | TBD | mA |
| | IDD2P ₂ | VDD2 | TBD | TBD | mA |
| | IDD2P _Q | VDDQ | TBD | TBD | mA |
| IDD2PS | IDD2PS ₁ | VDD1 | TBD | TBD | mA |
| | IDD2PS ₂ | VDD2 | TBD | TBD | mA |
| | IDD2PS _Q | VDDQ | TBD | TBD | mA |
| IDD2N | IDD2N ₁ | VDD1 | TBD | TBD | mA |
| | IDD2N ₂ | VDD2 | TBD | TBD | mA |
| | IDD2N _Q | VDDQ | TBD | TBD | mA |
| IDD2NS | IDD2NS ₁ | VDD1 | TBD | TBD | mA |
| | IDD2NS ₂ | VDD2 | TBD | TBD | mA |
| | IDD2NS _Q | VDDQ | TBD | TBD | mA |
| IDD3P | IDD3P ₁ | VDD1 | TBD | TBD | mA |
| | IDD3P ₂ | VDD2 | TBD | TBD | mA |
| | IDD3P _Q | VDDQ | TBD | TBD | mA |
| IDD3PS | IDD3PS ₁ | VDD1 | TBD | TBD | mA |
| | IDD3PS ₂ | VDD2 | TBD | TBD | mA |
| | IDD3PS _Q | VDDQ | TBD | TBD | mA |
| IDD3N | IDD3N ₁ | VDD1 | TBD | TBD | mA |
| | IDD3N ₂ | VDD2 | TBD | TBD | mA |
| | IDD3N _Q | VDDQ | TBD | TBD | mA |
| IDD3NS | IDD3NS ₁ | VDD1 | TBD | TBD | mA |
| | IDD3NS ₂ | VDD2 | TBD | TBD | mA |
| | IDD3NS _Q | VDDQ | TBD | TBD | mA |
| IDD4R | IDD4R ₁ | VDD1 | TBD | TBD | mA |
| | IDD4R ₂ | VDD2 | TBD | TBD | mA |
| | IDD4R _Q | VDDQ | TBD | TBD | mA |
| IDD4W | IDD4W ₁ | VDD1 | TBD | TBD | mA |
| | IDD4W ₂ | VDD2 | TBD | TBD | mA |
| | IDD4W _Q | VDDQ | TBD | TBD | mA |
| IDD5 | IDD5 ₁ | VDD1 | TBD | TBD | mA |
| | IDD5 ₂ | VDD2 | TBD | TBD | mA |
| | IDD5 _Q | VDDQ | TBD | TBD | mA |
| IDD5AB | IDD5AB ₁ | VDD1 | TBD | TBD | mA |
| | | VDD2 | TBD | TBD | mA |
| | | VDDQ | TBD | TBD | mA |

| Symbol | | Power Supply | 32Gb 2ch x32 | | Units | |
|--------|---------------------|--------------|--------------|----------|-------|----|
| | | | 3733Mbps | 4266Mbps | | |
| IDD5PB | IDD5PB ₁ | VDD1 | TBD | TBD | mA | |
| | IDD5PB ₂ | VDD2 | TBD | TBD | mA | |
| | IDD5PB _Q | VDDQ | TBD | TBD | mA | |
| IDD6 | IDD6 ₁ | VDD1 | 25°C | TBD | TBD | mA |
| | | | 95°C | TBD | TBD | |
| | IDD6 ₂ | VDD2 | 25°C | TBD | TBD | mA |
| | | | 95°C | TBD | TBD | |
| | IDD6 _Q | VDDQ | 25°C | TBD | TBD | mA |
| | | | 95°C | TBD | TBD | |

12 AC AND DC OUTPUT MEASUREMENT LEVELS

12.0 Single Ended AC and DC Output Levels

Table 55 shows the output levels used for measurements of single ended signals.

[Table 55] Single-ended AC and DC Output Levels

| Symbol | Parameter | Value | | | Unit | Notes |
|------------------|--------------------------------------|---------------------------|-----------------------|------------------------|------|-------|
| | | Under LPDDR4x-TBD Un-term | TBD to 3200 VSSQ term | 3200 to 4266 VSSQ term | | |
| V_{OH} (DC) | AC, DC output high measurement level | VDDQ | VDDQ/2 | VDDQ/2 | V | 1 |
| V_{OL} (DC) | AC, DC output low measurement level | VSSQ | VSSQ | VSSQ | V | |

NOTE :

1) 60ohm ODT value is assumed.

12.1 Pull Up/Pull Down Driver Characteristics and Calibration

[Table 56] Pull-down Driver Characteristics, with ZQ Calibration

| R _{ONPD,NOM} | Resistor | Min | Nom | Max | Unit |
|-----------------------|----------------------|------|------|------|-------------------|
| 40.0 Ohm | R _{ON40PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/6} |
| 48.0 Ohm | R _{ON48PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/5} |
| 60.0 Ohm | R _{ON60PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/4} |
| 80.0 Ohm | R _{ON80PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/3} |
| 120.0 Ohm | R _{ON120PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/2} |
| 240.0 Ohm | R _{ON240PD} | 0.90 | 1.00 | 1.10 | R _{ZQ/1} |

NOTE :

1) All values are after ZQ Calibration. Without ZQ Calibration RONPD values are ± 30%.

[Table 57] Pull-up Characteristics, with ZQ Calibration

| VOH _{PU, nom} | VOH,nom (mV) | Min | Nom | Max | Unit |
|------------------------|--------------|------|-----|------|---------|
| VDDQx0.5 | 300 | 0.90 | 1.0 | 1.10 | VOH,nom |
| VDDQx0.6 | 360 | 0.90 | 1.0 | 1.10 | VOH,nom |

NOTE :

1) All values are after ZQ Calibration. Without ZQ Calibration VOH(nom) values are ± 30%

2) VOH,nom (mV) values are based on a nominal VDDQ = 0.6V.

[Table 58] Valid Calibration Points

| VOH _{PU, nom} | ODT Value | | | | | |
|------------------------|-----------|-------|-------|-------|-------|-------|
| | 240 | 120 | 80 | 60 | 48 | 40 |
| VDDQx0.5 | VALID | VALID | VALID | VALID | VALID | VALID |
| VDDQx0.6 | DNU | VALID | DNU | VALID | DNU | DNU |

NOTE :

1) Once the output is calibrated for a given VOH(nom) calibration point, the ODT value may be changed without recalibration.

2) If the VOH(nom) calibration point is changed, then re-calibration is required.

3) DNU = Do Not Use.

[Table 59] Pull-down Characteristics without ZQ Calibration

| R _{ONPD,NOM} | Resistor | V _{out} | Min | Nom | Max | Unit | Notes |
|-----------------------|---------------------|-----------------------|------|------|------|-------------------|-------|
| 40.0Ω | R _{ON40PD} | 0.5 × V _{OH} | 0.70 | 1.00 | 1.30 | R _{ZQ/6} | 1 |
| 48.0Ω | R _{ON48PD} | 0.5 × V _{OH} | 0.70 | 1.00 | 1.30 | R _{ZQ/5} | 1 |

NOTE:

1) Across entire operating temperature range, without calibration.

[Table 60] Pull-up Characteristics without V_{OH} Calibration (Die to Die)

| VOH _{PU, (nom)} | VOH(nom) (mV) | Variation | | | Unit | Notes |
|--------------------------|---------------|-----------|-----|------|----------|-------|
| | | Min | Nor | Max | | |
| VDDQx0.5 | 300 | 0.70 | 1.0 | 1.30 | VOH(nom) | 1 |
| VDDQx0.6 | 360 | 0.70 | 1.0 | 1.30 | VOH(nom) | 1 |

NOTE :

1) ODT value of Memory controller should be informed with MRW before V_{OH} calibration.

[Table 61] V_{OUT} level of un-terminated condition

| Parameter | Symbol | Min | Max | Unit | Note |
|---|------------------------|-----------|-----------|------|------|
| Output High voltage level when ODT of memory controller is turned off | V _{OH_unterm} | VDDQ-0.55 | VDDQ-0.15 | V | |

13 ELECTRICAL CHARACTERISTICS AND ACTIMING

13.1 Clock Specification

The jitter specified is a random jitter meeting a Gaussian distribution. Input clocks violating the min/max values may result in malfunction of the LPDDR4x device.

13.1.1 Definition for tCK(avg and nCK)

tCK(avg) is calculated as the average clock period across any consecutive 200 cycle window, where each clock period is calculated from rising edge to rising edge.

$$tCK(avg) = \left(\sum_{j=1}^N tCK_j \right) / N$$

where $N = 200$

Unit 'tCK(avg)' represents the actual clock average tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.

tCK(avg) may change by up to +/-1% within a 100 clock cycle window, provided that all jitter and timing specs are met.

13.1.2 Definition for tCK(abs)

tCK(abs) is defined as the absolute clock period, as measured from one rising edge to the next consecutive rising edge.

tCK(abs) is not subject to production test.

13.1.3 Definition for tCH(avg) and tCL(avg)

tCH(avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left(\sum_{j=1}^N tCH_j \right) / (N \times tCK(avg))$$

where $N = 200$

tCL(avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left(\sum_{j=1}^N tCL_j \right) / (N \times tCK(avg))$$

where $N = 200$

13.1.4 Definition for tCH(abs) and tCL(abs)

tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.

tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.

Both tCH(abs) and tCL(abs) are not subject to production test.

13.1.5 Definition for tJIT(per)

tJIT(per) is the single period jitter defined as the largest deviation of any signal tCK from tCK(avg).

tJIT(per) = Min/max of {tCK_i - tCK(avg) where i = 1 to 200}.

tJIT(per)_{act} is the actual clock jitter for a given system.

tJIT(per)_{allowed} is the specified allowed clock period jitter.

tJIT(per) is not subject to production test.

13.1.6 Definition for tJIT(cc)

tJIT(cc) is defined as the absolute difference in clock period between two consecutive clock cycles.

$$t_{JIT(cc)} = \text{Max of } |t_{CK(i+1)} - t_{CK(i)}|.$$

tJIT(cc) defines the cycle to cycle jitter.

tJIT(cc) is not subject to production test.

13.1.7 Definition for tERR(nper)

tERR(nper) is defined as the cumulative error across n multiple consecutive cycles from tCK(avg).

tERR(nper)_{act} is the actual clock jitter over n cycles for a given system.

tERR(nper)_{allowed} is the specified allowed clock period jitter over n cycles.

tERR(nper) is not subject to production test.

$$tERR(nper) = \left(\sum_{j=i}^{i+n-1} tCK_j \right) - n \times tCK(avg)$$

tERR(nper)_{min} can be calculated by the formula shown below:

$$tERR(nper), min = (1 + 0.68 LN(n)) \times tJIT(per), min$$

tERR(nper)_{max} can be calculated by the formula shown below

$$tERR(nper), max = (1 + 0.68 LN(n)) \times tJIT(per), max$$

Using these equations, tERR(nper) tables can be generated for each tJIT(per)_{act} value.

13.1.8 Definition for duty cycle jitter tJIT(duty)

tJIT(duty) is defined with absolute and average specification of tCH / tCL.

$$tJIT(duty), min = MIN((tCH(abs), min - tCH(avg), min), (tCL(abs), min - tCL(avg), min)) \times tCK(avg)$$

$$tJIT(duty), max = MAX((tCH(abs), max - tCH(avg), max), (tCL(abs), max - tCL(avg), max)) \times tCK(avg)$$

13.1.9 Definition for tCK(abs), tCH(abs) and tCL(abs)

These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times.

[Table 62] Definition for tCK(abs), tCH(abs), and tCL(abs)

| Parameter | Symbol | Min | Unit |
|---------------------------------|----------|---|----------|
| Absolute Clock Period | tCK(abs) | tCK(avg) _{min} + tJIT(per) _{min} | ps |
| Absolute Clock HIGH Pulse Width | tCH(abs) | tCH(avg) _{min} + tJIT(duty) _{min} / tCK(avg) _{min} | tCK(avg) |
| Absolute Clock LOW Pulse Width | tCL(abs) | tCL(avg) _{min} + tJIT(duty) _{min} / tCK(avg) _{min} | tCK(avg) |

NOTE :

1) tCK(avg)_{min} is expressed in ps for this table.

2) tJIT(duty)_{min} is a negative value.

13.2 Period Clock Jitter

LPDDR4x devices can tolerate some clock period jitter without core timing parameter de-rating. This section describes device timing requirements in the presence of clock period jitter (tJIT(per)) in excess of the values found in Table 62, LPDDR4x AC Timing Table and how to determine cycle time derating and clock cycle de-rating.

13.2.1 Clock period jitter effects on core timing parameters

(tRCD, tRP, tRTP, tWR, tWRA, tWTR, tRC, tRAS, tRRD, tFAW)

Core timing parameters extend across multiple clock cycles. Period clock jitter will impact these parameters when measured in numbers of clock cycles. When the device is operated with clock jitter within the specification limits, the LPDDR4x device is characterized and verified to support $tnPARAM = RU\{tPARAM / tCK(avg)\}$.

When the device is operated with clock jitter outside specification limits, the number of clocks or tCK(avg) may need to be increased based on the values for each core timing parameter.

13.2.1.1 Cycle time de-rating for core timing parameters

For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the amount of cycle time de-rating (in ns) required if the equation results in a positive value for a core timing parameter.

$$CycleTimeDerating = MAX\left\{\left(\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tnPARAM} - tCK(avg)\right), 0\right\}$$

A cycle time derating analysis should be conducted for each core timing parameter. The amount of cycle time derating required is the maximum of the cycle time de-ratings determined for each individual core timing parameter.

13.2.1.2 Clock Cycle de-rating for core timing parameters

For a given number of clocks (tnPARAM) for each core timing parameter, clock cycle de-rating should be specified with amount of period jitter (tJIT(per)). For a given number of clocks (tnPARAM), for each core timing parameter, average clock period (tCK(avg)) and actual cumulative period error (tERR(tnPARAM),act) in excess of the allowed cumulative period error (tERR(tnPARAM),allowed), the equation below calculates the clock cycle derating (in clocks) required if the equation results in a positive value for a core timing parameter.

$$ClockCycleDerating = RU\left\{\frac{tPARAM + tERR(tnPARAM), act - tERR(tnPARAM), allowed}{tCK(avg)}\right\} - tnPARAM$$

A clock cycle de-rating analysis should be conducted for each core timing parameter.

13.2.2 Clock jitter effects on Command/Address timing parameters

Command/address timing parameters (tIS, tIH, tISb, tIHb) are measured from a command/address signal (CS or CA[5:0]) transition edge to its respective clock signal (CK_t/ CK_c) crossing. The specification values are not affected by the tJIT(per) applied, because the setup and hold times are relative to the clock signal crossing that latches the command/address. Regardless of clock jitter values, these values must be met.

13.2.3 Clock jitter effects on Read timing parameters

13.2.3.1 tRPRE

When the device is operated with input clock jitter, tRPRE needs to be de-rated by the actual period jitter (tJIT(per),act,max) of the input clock in excess of the allowed period jitter (tJIT(per),allowed,max). Output de-ratings are relative to the input clock.

$$tRPRE(min, derated) = 0.9 - \left(\frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK(avg)} \right)$$

For example,

if the measured jitter into a LPDDR4x device has tCK(avg) = 625ps, tJIT(per),act,min = -xx, and tJIT(per),act,max = +xx ps, then tRPRE,min,derated = 0.9 - (tJIT(per),act,max - tJIT(per),allowed,max)/tCK(avg) = 0.9 - (xx - xx)/xx = yy tCK(avg).

13.2.3.2 tLZ(DQ), tHZ(DQ), tDQSCK, tLZ(DQS), tHZ(DQS)

These parameters are measured from a specific clock edge to a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition and will be met with respect to that clock edge. Therefore, they are not affected by the amount of clock jitter applied (i.e. tJIT(per)).

13.2.3.3 tQSH, tQSL

These parameters are affected by duty cycle jitter which is represented by tCH(abs)min and tCL(abs)min.

These parameters determine absolute Data-Valid window(DVW) at the LPDDR4x device pin.

Absolute min DVW @LPDDR4x device pin = min { (tQSH(abs)min – tDQSQmax), (tQSL(abs)min – tDQSQmax) }

This minimum DVW shall be met at the target frequency regardless of clock jitter.

13.2.3.4 tRPST

tRPST is affected by duty cycle jitter which is represented by tCL(abs). Therefore tRPST(abs)min can be specified by tCL(abs)min.

tRPST(abs)min = tCL(abs)min – 0.05 = tQSL(abs)min

13.2.4 Clock jitter effects on Write timing parameters

13.2.4.1 tDS, tDH

These parameters are measured from a data signal (DMn, DQm.: n=0,1,2,3. m=0 –31) transition edge to its respective data strobe signal (DQS_n_t, DQS_n_c : n=0,1,2,3) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold are relative to the data strobe signal crossing that latches the data. Regardless of clock jitter values, these values shall be met.

13.2.4.2 tDSS, tDSH

These parameters are measured from a data strobe signal (DQS_x_t, DQS_x_c) crossing to its respective clock signal (CK_t/CK_c) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per)), as the setup and hold of the data strobes are relative to the corresponding clock signal crossing. Regardless of clock jitter values, these values shall be met.

13.2.4.3 tDQSS

This parameter is measured from a data strobe signal (DQSx_t, DQSx_c) crossing to the subsequent clock signal (CK_t/CK_c) crossing. When the device is operated with input clock jitter, this parameter needs to be de-rated by the actual period jitter tJIT(per),act of the input clock in excess of the allowed period jitter tJIT(per),allowed.

$$tDQSS (min, derated) = 0.75 - \frac{tJIT(per), act, min - tJIT(per), allowed, min}{tCK (avg)}$$

$$tDQSS (max, derated) = 1.25 - \frac{tJIT(per), act, max - tJIT(per), allowed, max}{tCK (avg)}$$

For example,

if the measured jitter into an LPDDR4x device has tCK(avg) = 625ps, tJIT(per),act,min = -xxps, and tJIT(per),act,max = +xx ps, then:

tDQSS,(min,derated) = 0.75 - (-xx + yy)/625 = xxxx tCK(avg)

tDQSS,(max,derated) = 1.25 - (xx . yy)/625 = xxxx tCK(avg)

13.3 LPDDR4x Refresh Requirements

[Table 63] LPDDR4x Refresh Requirement Parameters per die for Single Channel SDRAM devices

| Parameter | Symbol | 8Gb/16Gb | 32Gb | unit | |
|---|----------------------|---------------------------------|-------|-------|----|
| Density per Channel | | 8Gb | 16Gb | | |
| Number of Banks per Channel | | 8 | 8 | | |
| Refresh Window Tcase ≤ 85°C | t _{REFW} | 32 | 32 | ms | |
| Refresh Window 1/2-Rate Refresh | t _{REFW} | 16 | 16 | ms | |
| Refresh Window 1/4-Rate Refresh | t _{REFW} | 8 | 8 | ms | |
| Required number of REFRESH commands in a t _{REFW} window (min) | R | 8,192 | 8192 | | |
| Average Refresh Interval | REFab | t _{REFI} ³⁾ | 3.904 | 3.904 | us |
| | REFpb | t _{REFIpb} | 488 | 488 | us |
| Refresh Cycle time (All Banks) | t _{RFCab} | 280 | 380 | ns | |
| Refresh Cycle time (Per Bank) | t _{RFCpb} | 140 | 190 | ns | |
| Per-bank Refresh to Per-bank Refresh different bank Time | t _{pbR2pbR} | 90 | 90 | ns | |

NOTE :

1) Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.

2) Self refresh abort feature is available for higher density devices starting with 12Gb dual channel device and 6Gb single channel device and tXSR_abort(min) is defined as tRFCpb + 17.5ns.

3) t_{REFI} values for all bank refresh is Tc = -40~85°C, Tc means Operating Case Temperature.

13.4 AC Timing

[Table 64] LPDDR4x AC Timing Table

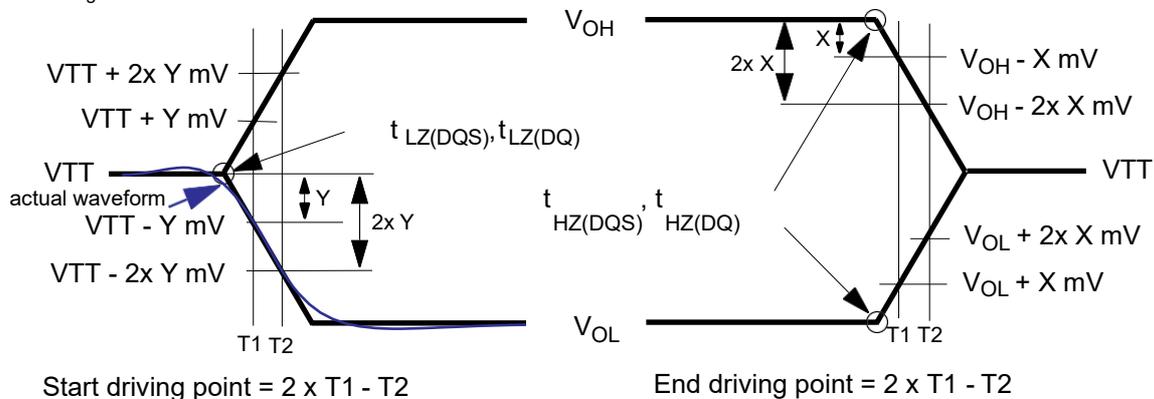
| Parameter | Symbol | Min/ Max | LPDDR4x | | | Unit |
|---|--------------------------|----------|---|----------|----------|---------------|
| | | | 3200Mbps | 3733Mbps | 4266Mbps | |
| Maximum clock frequency | | ~ | 1600 | 1866 | 2133 | MHz |
| Clock Timing | | | | | | |
| Average Clock Period | $t_{CK(avg)}$ | MIN | 0.625 | 0.536 | 0.468 | ns |
| | | MAX | 100 | | | |
| Average HIGH pulse width | $t_{CH(avg)}$ | MIN | 0.45 | | | $t_{CK(avg)}$ |
| | | MAX | 0.55 | | | |
| Average LOW pulse width | $t_{CL(avg)}$ | MIN | 0.45 | | | $t_{CK(avg)}$ |
| | | MAX | 0.55 | | | |
| Absolute clock period | $t_{CK(abs)}$ | MIN | $t_{CK(avg)} \text{ MIN} + t_{JIT(per)} \text{ MIN}$ | | | ns |
| Absolute HIGH clock pulse width | $t_{CH(abs)}$ | MIN | 0.43 | | | $t_{CK(avg)}$ |
| | | MAX | 0.57 | | | |
| Absolute LOW clock pulse width | $t_{CL(abs)}$ | MIN | 0.43 | | | $t_{CK(avg)}$ |
| | | MAX | 0.57 | | | |
| Clock period jitter | $t_{JIT(per)}$ | MIN | -40 | -36 | -30 | ps |
| | | MAX | 40 | 36 | 30 | |
| Maximum Clock Jitter between two consecutive cycles | $t_{JIT(cc)}$ | MAX | 80 | 72 | 60 | ps |
| Duty cycle jitter (with supported jitter) | $t_{JIT(duty); allowed}$ | MIN | $\min((t_{CH(abs),min} - t_{CH(avg),min}), (t_{CL(abs),min} - t_{CL(avg),min})) \times t_{CK(avg)}$ | | | ps |
| | | MAX | $\max((t_{CH(abs),max} - t_{CH(avg),max}), (t_{CL(abs),max} - t_{CL(avg),max})) \times t_{CK(avg)}$ | | | |
| Core Parameters ¹⁷⁾ | | | | | | |
| READ latency (no DBI) | RL | MIN | 28 | 32 | 36 | $t_{CK(avg)}$ |
| WRITE latency (set A) | WL | MIN | 14 | 16 | 18 | $t_{CK(avg)}$ |
| ACTIVATE-to-ACTIVATE command period (same bank) | t_{RC} | MIN | $t_{RAS} + t_{RPab}$ (with all-bank precharge) $t_{RAS} + t_{RPpb}$ (with per-bank precharge) | | | ns |
| Minimum Self-Refresh Time (Entry to Exit) | t_{SR} | MIN | $\max(15ns, 3t_{CK})$ | | | ns |
| SELF REFRESH exit to next valid command delay | t_{XSR} | MIN | $\text{Max}(t_{RFCab} + 7.5ns, 2t_{CK})$ | | | ns |
| Exit power down to next valid command delay | t_{XP} | MIN | $\text{Max}(7.5ns, 5t_{CK})$ | | | ns |
| CAS-to-CAS delay | t_{CCD} | MIN | BL/2 | | | $t_{CK(avg)}$ |
| CAS to CAS delay Masked Write | $t_{CCDMW}^{31)}$ | MIN | $4 \times t_{CCD}$ | | | $t_{CK(avg)}$ |
| Internal READ to PRECHARGE command delay | t_{RTP} | MIN | $\text{Max}(7.5ns, 8t_{CK})$ | | | ns |
| RAS-to-CAS delay | t_{RCD} | MIN | $\text{Max}(18ns, 4t_{CK})$ | | | ns |
| Row Precharge Time (single bank) | t_{RPpb} | MIN | $\text{Max}(18ns, 4t_{CK})$ | | | ns |
| Row Precharge Time (all banks) | t_{RPab} | MIN | $\text{Max}(21ns, 4t_{CK})$ | | | ns |
| Row active time | t_{RAS} | MIN | $\text{Max}(42ns, 3t_{CK})$ | | | ns |
| | | MAX | $\min(9 \times t_{REFI} \times \text{Refresh Rate}^{19}), 70.2)$ | | | us |
| WRITE recovery time | t_{WR} | MIN | $\text{Max}(18ns, 6t_{CK})$ | | | ns |
| WRITE-to-READ delay | t_{WTR} | MIN | $\text{Max}(10ns, 8t_{CK})$ | | | ns |
| Active bank-A to Active bank-B | t_{RRD} | MIN | $\text{Max}(10ns, 4t_{CK})$ | | | ns |
| Precharge to Precharge Delay | t_{PPD} | MIN | 4 | | | tCK |
| Four-bank ACTIVATE Window | t_{FAW} | MIN | 40 | | | ns |
| CKE minimum pulse width during SELF REFRESH (low pulse width during SELF REFRESH) | t_{CKELPD} | MIN | $\text{Max}(7.5ns, 3t_{CK})$ | | | ns |

| Parameter | Symbol | Min/ Max | LPDDR4x | | | Unit |
|---|----------------------------------|-------------|---|----------|----------|---------------|
| | | | 3200Mbps | 3733Mbps | 4266Mbps | |
| READ Parameters⁴⁾ | | | | | | |
| Read preamble | $t_{RPRE}^{5), 8)}$ | MIN | 2.0 | | | $t_{CK}(avg)$ |
| 0.5 tCK Read postamble | $t_{RPST}^{5), 9)}$ | MIN | 0.5 | | | $t_{CK}(avg)$ |
| 1.5 tCK Read postamble | t_{RPST} | MIN | 1.5 | | | $t_{CK}(avg)$ |
| DQ low-impedance time from CK_t, CK_c | $t_{LZ(DQ)}^{5)}$ | MIN | $(RL \times t_{CK}) + t_{DQSK(Min)} - 200ps$ | | | ps |
| DQ high impedance time from CK_t, CK_c | $t_{HZ(DQ)}^{5)}$ | MAX | $(RL \times t_{CK}) + t_{DQSK(Max)} + t_{DQSQ(Max)} + (BL/2 \times t_{CK}) - 100ps$ | | | ps |
| DQS_c low-impedance time from CK_t, CK_c | $t_{LZ(DQS)}^{5)}$ | MIN | $(RL \times t_{CK}) + t_{DQSK(Min)} - (t_{PRE(Max)} \times t_{CK}) - 200ps$ | | | ps |
| DQS_c high impedance time from CK_t, CK_c | $t_{HZ(DQS)}^{5)}$ | MAX | $(RL \times t_{CK}) + t_{DQSK(Max)} + (BL/2 \times t_{CK}) - (RPST(Max) \times t_{CK}) - 100ps$ | | | ps |
| DQS-DQ skew | t_{DQSQ} | MAX | 0.18 | | | UI |
| tDQSK Parameters | | | | | | |
| DQS output access time from CK_t/CK_c | $t_{DQSK}^{14)}$ | MIN | 1500 | | | ps |
| | | MAX | 3500 | | | |
| DQS output access time from CK_t/CK_c temperature variation | $t_{DQSK_temp}^{15)}$ | MAX | 4 | | | ps/°C |
| DQS output access time from CK_t/CK_c voltage variation | $t_{DQSK_volt}^{16)}$ | MAX | 7 | | | ps/mV |
| CK to DQS rank to rank variation | $t_{DQSK_rank2rank}^{22), 23)}$ | MAX | 1.0 | | | ns |
| Self Refresh Parameters | | | | | | |
| Delay from SRE command to CKE Input low | $t_{ESCKE}^{24)}$ | MIN | Max(1.75ns, 3nCK) | | | ns |
| Minimum Self Refresh Time | $t_{SR}^{24)}$ | MIN | Max(15ns, 3tCK) | | | ns |
| Exit Self Refresh to Valid commands | $t_{XSR}^{24), 25)}$ | MIN | Max(tRFCab + 7.5ns, 2tCK) | | | ns |
| WRITE Parameters⁴⁾ | | | | | | |
| Write command to 1 st DQS latching | t_{DQSS} | MIN | 0.75 | | | $t_{CK}(avg)$ |
| | | MAX | 1.25 | | | |
| DQS input high-level width | t_{DQSH} | MIN | 0.4 | | | $t_{CK}(avg)$ |
| DQS input low-level width | t_{DQSL} | MIN | 0.4 | | | $t_{CK}(avg)$ |
| DQS falling edge to CK setup time | t_{DSS} | MIN | 0.2 | | | $t_{CK}(avg)$ |
| DQS falling edge hold time from CK | t_{DSH} | MIN | 0.2 | | | $t_{CK}(avg)$ |
| Write preamble | t_{WPRE} | MIN | 2.0 | | | $t_{CK}(avg)$ |
| 0.5 tCK Write postamble | $t_{WPST}^{21)}$ | MIN | 0.5 | | | $t_{CK}(avg)$ |
| 1.5 tCK Write postamble | $t_{WPST}^{21)}$ | MIN | 1.5 | | | $t_{CK}(avg)$ |
| ZQ Calibration Parameters | | | | | | |
| ZQ Calibration | t_{ZQCAL} | MIN | 1 | | | us |
| ZQ Calibration Values Latch Time | t_{ZQLAT} | MIN | Max(30ns, 8tCK) | | | ns |
| ZQ Calibration RESET time | $t_{ZQRESET}$ | MIN | Max(50ns, 3tCK) | | | ns |
| Power Down Parameters | | | | | | |
| CKE minimum pulse width (HIGH and LOW pulse width) | t_{CKE} | MIN | max(7.5ns, 4tCK) | | | ns |
| Delay from Valid command to CKE Input low | $t_{CMDCKE}^{26)}$ | MIN | Max(1.75ns, 3tCK) | | | ns |
| Valid Clock Requirement after CKE Input Low | $t_{CKELCK}^{26)}$ | MIN | Max(5ns, 5tCK) | | | - |
| Valid CS Requirement before CKE Input Low | t_{CSCKE} | MIN | 1.75 | | | ns |
| Valid CS Requirement after CKE Input Low | t_{CKELCS} | MIN | Max(5ns, 5tCK) | | | ns |

| Parameter | Symbol | Min/ Max | LPDDR4x | | | Unit |
|---|---------------------|-------------|---|----------|----------|------|
| | | | 3200Mbps | 3733Mbps | 4266Mbps | |
| Valid Clock Requirement before CKE Input High | $t_{CKCKEH}^{26)}$ | MIN | Max(1.75ns, 3tCK) | | | -ns |
| Exit power- down to next valid command delay | $t_{XP}^{26)}$ | MIN | Max(7.5ns, 5tCK) | | | ns |
| Valid CS Requirement before CKE Input High | t_{CSCKEH} | MIN | 1.75 | | | ns |
| Valid CS Requirement after CKE Input High | t_{CKEHCS} | MIN | Max(7.5ns,5tCK) | | | ns |
| Valid Clock and CS Requirement after CKE Input low after MRW Command | $t_{MRWCKEL}^{26)}$ | MIN | Max(14ns,10tCK) | | | ns |
| Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command | $t_{ZQCKE}^{26)}$ | MIN | Max(1.75ns,3tCK) | | | ns |
| Command Address Input Parameters ⁴⁾ | | | | | | |
| Rx Mask voltage - p-p | VcIVW | MAX | 155 | 150 | 145 | mV |
| Rx timing window | TcIVW | MAX | 0.3 | | | UI* |
| CA AC input pulse amplitude pk-pk | VIHL_AC | MIN | 190 | 180 | | mV |
| CA input pulse width | TcIPW | MIN | 0.6 | | | UI* |
| Input Slew Rate over VcIVW | SRIN_cIVW | MIN | 1 | | | V/ns |
| | | MAX | 7 | | | |
| Mode Register Read/Write AC Timing | | | | | | |
| Additional time after tXP has expired until MRR command | t_{MRRi} | MIN | $t_{RCD} + 3nCK$ | | | - |
| MODE REGISTER READ command period | t_{MRR} | MIN | 8 | | | nCK |
| MODE REGISTER WRITE command period | t_{MRW} | MIN | Max(10ns, 10nCK) | | | - |
| Mode register set command delay | t_{MRD} | MIN | Max(14ns, 10tCK) | | | - |
| Boot Parameters (10 MHz - 55 MHz) ^{11), 12), 13)} | | | | | | |
| Clock Cycle Time | t_{CKb} | max | 100 | | | ns |
| | | MIN | 18 | | | |
| Address & Control Input Setup Time | t_{ISb} | MIN | 1150 | | | ps |
| Address & Control Input Hold Time | t_{IHb} | MIN | 1150 | | | ps |
| DQS Output Data Access Time from CK_t/CK_c | t_{DQSCb} | MIN | 2.0 | | | ns |
| | | MAX | 10.0 | | | |
| Data Strobe Edge to Output Data Edge | t_{DQSQb} | MAX | 1.2 | | | ns |
| Command Bus Training AC Parameters | | | | | | |
| Valid Clock Requirement after CKE Input low | t_{CKELCK} | MIN | Max(5ns, 5nCK) | | | tCK |
| Data Setup for VREF Training Mode | $t_{DStrain}$ | MIN | 2 | | | ns |
| Data Hold for VREF Training Mode | $t_{DHtrain}$ | MIN | 2 | | | ns |
| Asynchronous Data Read | t_{ADR} | MAX | 20 | | | ns |
| CA Bus Training command to CA Bus Training command delay | $t_{CACD}^{29)}$ | MIN | RU(t_{ADR}/t_{CK}) | | | tCK |
| Valid Strobe Requirement before CKE Low | $t_{DQSCKE}^{30)}$ | MIN | 10 | | | ns |
| First CA Bus Training Command Following CKE LOW | t_{CAENT} | MIN | 250 | | | ns |
| VREF Step Time-multiple steps | t_{VREFCA_LONG} | MAX | 250 | | | ns |
| VREF Step Time-one step | t_{VREFCA_SHORT} | MAX | 80 | | | ns |
| Valid Clock Requirement before CS High | $t_{CKPRECS}$ | MIN | $2t_{CK} + t_{XP}$ ($t_{XP} = \max(7.5ns, 5nCK)$) | | | - |
| Valid Clock Requirement after CS High | $t_{CKPSTCS}$ | MIN | $\max(7.5ns, 5nCK)$ | | | - |
| Minimum delay from CS to DQS toggle in command bus training | t_{CS_VREF} | MIN | 2 | | | tCK |
| Minimum delay from CKE High to Strobe High Impedance | $t_{CKEHDQS}$ | - | 10 | | | ns |
| Valid Clock Requirement before CKE Input High | t_{CKCKEH} | MIN | Max(1.75ns, 3tCK) | | | |
| CA Bus Training CKE High to DQ Tri-state | t_{MRZ} | MIN | 1.5 | | | ns |

| Parameter | Symbol | Min/ Max | LPDDR4x | | | Unit |
|---|--------------------|-------------|-------------------|----------|----------|------|
| | | | 3200Mbps | 3733Mbps | 4266Mbps | |
| ODT turn-on Latency from CKE | $t_{CKELODTON}$ | MIN | 20 | | | ns |
| ODT turn-off Latency from CKE | $t_{CKELODTOFF}$ | MIN | 20 | | | ns |
| Exit Command Bus Training Mode to next valid command delay ³²⁾ | t_{XCBT_Short} | MIN | Max(5nCK, 200ns) | | | - |
| | t_{XCBT_Middle} | MIN | Max(5nCK, 200ns) | | | - |
| | t_{XCBT_Long} | MIN | Max(5nCK, 250ns) | | | - |
| Write Leveling Parameters | | | | | | |
| DQS_t/DQS_c delay after write leveling mode is programmed | $t_{WLDQSEN}$ | MIN | 20 | | | tCK |
| Write preamble for Write Leveling | t_{WLWPRE} | MIN | 20 | | | tCK |
| First DQS_t/DQS_c edge after write leveling mode is programmed | t_{WLMRD} | MIN | 40 | | | tCK |
| Write leveling output delay | t_{WLO} | MAX | 20 | | | ns |
| Mode register set command delay | t_{MRD} | MIN | Max(14ns, 10tCK) | | | ns |
| Valid Clock Requirement before DQS Toggle | $t_{CKPRDQS}$ | MIN | Max(7.5ns, 4tCK) | | | - |
| Valid Clock Requirement after DQS Toggle | $t_{CKPSTDQS}$ | MIN | Max(7.5ns, 4tCK) | | | - |
| Write leveling hold time | $t_{WLH}^{27)}$ | MIN | 75 | 60 | 50 | ps |
| Write leveling setup time | $t_{WLS}^{27)}$ | MIN | 75 | 60 | 50 | ps |
| Write leveling input valid window | $t_{WLIVW}^{28)}$ | MIN | 120 | 100 | 90 | ps |
| Temperature De-Rating AC Timing ²⁰⁾ | | | | | | |
| DQS output access time from CK_t/CK_c (derated) | t_{DQSCK} | MAX | 3600 | | | ps |
| RAS-to-CAS delay (derated) | t_{RCD} | MIN | $t_{RCD} + 1.875$ | | | ns |
| ACTIVATE-to- ACTIVATE command period (derated) | t_{RC} | MIN | $t_{RC} + 3.75$ | | | ns |
| Row active time (derated) | t_{RAS} | MIN | $t_{RAS} + 1.875$ | | | ns |
| Row precharge time (derated) | t_{RP} | MIN | $t_{RP} + 1.875$ | | | ns |
| Active bank A to active bank B (derated) | t_{RRD} | MIN | $t_{RRD} + 1.875$ | | | ns |

- NOTE :**
- 1) Frequency values are for reference only. Clock cycle time (tCK) is used to determine device capabilities.
 - 2) All AC timings assume an input slew rate of TBDV/ns.
 - 3) Measured with 4 V/ns differential CK_t/CK_c slew rate and nominal VIX.
 - 4) READ, WRITE, and Input setup and hold times are referenced to V_{REF}.
 - 5) For LOW-to-HIGH and HIGH-to-LOW transitions, the timing reference is at the point when the signal crosses the transition threshold (V_{TT}). tHZ and tLZ transitions occur in the same access time (with respect to clock) as valid data transitions. These parameters are not referenced to a specific voltage level but to the time when the device output is no longer driving (for tRPST, tHZ(DQS) and tHZ(DQ)), or begins driving (for tRPRE, tLZ(DQS), tLZ(DQ)). Operating and Timing [Burst Read:RL=12, BL=8, tDQSK<tCK] shows a method to calculate the point when device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent.
 - 6) Output Transition Timing



- 7) The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single-ended. The timing parameters tRPRE and tRPST are determined from the differential signal DQS_t-DQS_c.
- 8) Measured from the point when DQS_t/DQS_c begins driving the signal to the point when DQS_t/DQS_c begins driving the first rising strobe edge. See Pre and Post-amble section in Operating & Timing spec
- 9) Measured from the last falling strobe edge of DQS_t/DQS_c to the point when DQS_t/DQS_c finishes driving the signal.
- 10) Input set-up/hold time for signal (CA[9:0], CS).
- 11) To ensure device operation before the device is configured, a number of AC boot-timing parameters are defined in this table. Boot parameter symbols have the letter b appended (for example, tCK during boot is tCKb).
- 12) The LPDDR4x device will set some default values upon receiving a RESET (MRW) command as specified in "Definition".

- 13) The output skew parameters are measured with default output impedance settings using the reference load.
- 14) Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies > 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
- 15) tDQSKCK_temp max delay variation as a function of Temperature.
- 16) tDQSKCK_volt max delay variation as a function of DC voltage variation for VDDQ and VDD2. tDQSKCK_volt should be used to calculate timing variation due to VDDQ and VDD2 noise < 20 MHz. Host controller do not need to account for any variation due to VDDQ and VDD2 noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the $\text{Max}\{\text{abs}\{tDQSKCK_{min}@V1-tDQSKCK_{max}@V2\}, \text{abs}\{tDQSKCK_{max}@V1-tDQSKCK_{min}@V2\}\}/\text{abs}\{V1-V2\}$.
- 17) Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
- 18) tXSR/tXP/tZQLAT are defined as "to the first rising clock edge next valid command".
- 19) Refresh Rate is specified by MR4, OP[2:0].
- 20) Timing derating applies for operation at 85°C to 105°C.
- 21) The length of Write Postamble depends on MR3 OP1 setting.
- 22) The same voltage and temperature are applied to tDQS2CK_rank2rank.
- 23) tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
- 24) Delay time has to satisfy both analog time(ns) and clock count(tCK).

It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3tCK is applied to is shown below.

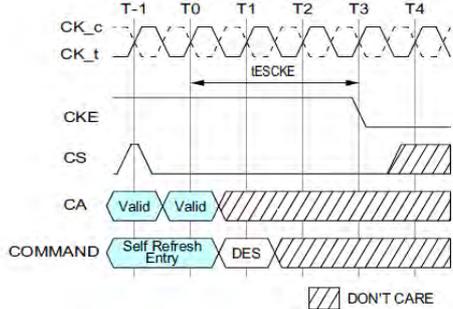


Figure 24. tESCKE Timing

- 25) MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.
 - 26) Delay time has to satisfy both analog time(ns) and clock count(nCK).
- For example, tCMDCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired. The case which 3nCK is applied to is shown below.

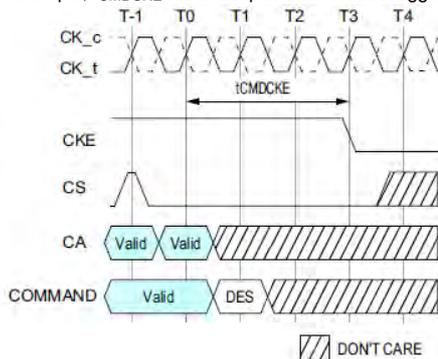


Figure 25. tCMDCKE Timing

- 27) In addition to the traditional setup and hold time specifications above, there is value in an input valid window based specification for write-leveling training. As the training is based on each device, worst case process skews for setup and hold do not make sense to close timing between CK and DQS.
 - 28) tWLIVW is defined in a similar manner to tDIVW_Total, except that here it is a DQS input valid window with respect to CK. This would need to account for all VT (voltage and temperature) drift terms between CK and DQS within the DRAM that affect the write-leveling input valid window.
- The DQS input mask for timing with respect to CK is shown in Figure 26. The "total" mask (tWLIVW) defines the time the input signal must not encroach in order for the DQS input to be successfully captured by CK with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

DQS_t/DQS_c and CK_t/CK_c at DRAM Latch

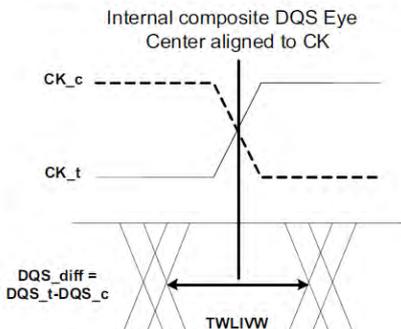


Figure 26. DQS_t/DQS_c to CK_t/CK_c timings at the DRAM pins referenced from the internal latch

- 29) If tACAD is violated, the data for samples which violate tACAD will not be available, except for the last sample (where tACAD after this sample is met). Valid data for the last sample will be available after tADR.
- 30) DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
- 31) See Masked Write Operation for detail.
- 32) Precharge to precharge timing restriction does not apply to Auto-Precharge commands.
- 33) Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. The details are shown in tFC value mapping table. Additionally, exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Setting time of VREF(DQ) level is same as VREF(CA) level.

13.5 CA Rx Voltage and Timing

The command and address (CA) including CS input receiver compliance mask for voltage and timing is shown in the figure below. All CA, CS signals apply the same compliance mask and operate in single data rate mode.

The CA input receiver mask for voltage and timing is shown in the figure below is applied across all CA pins. The receiver mask (Rx Mask) defines the area that the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

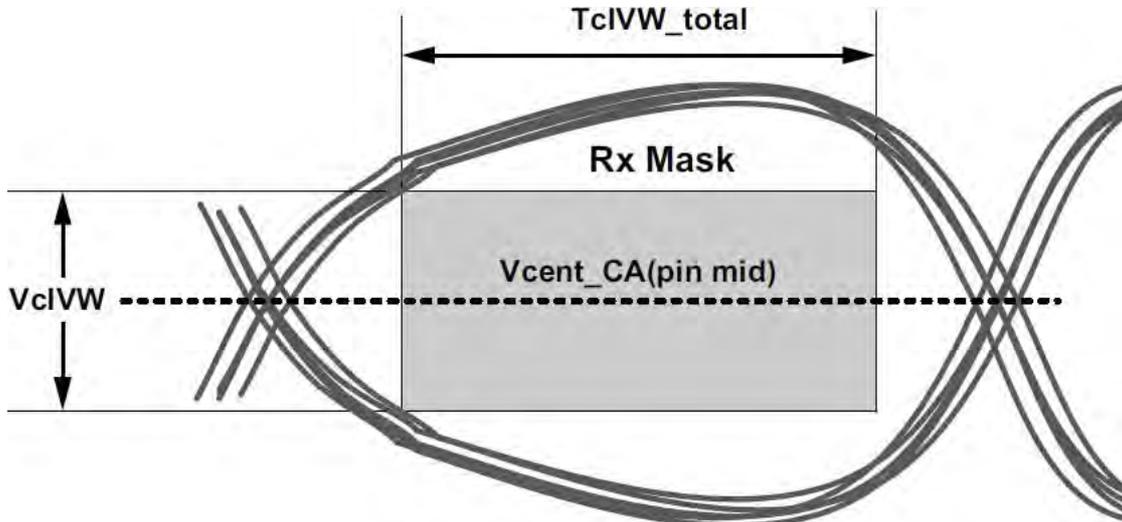


Figure 27. CA Receiver (Rx) mask

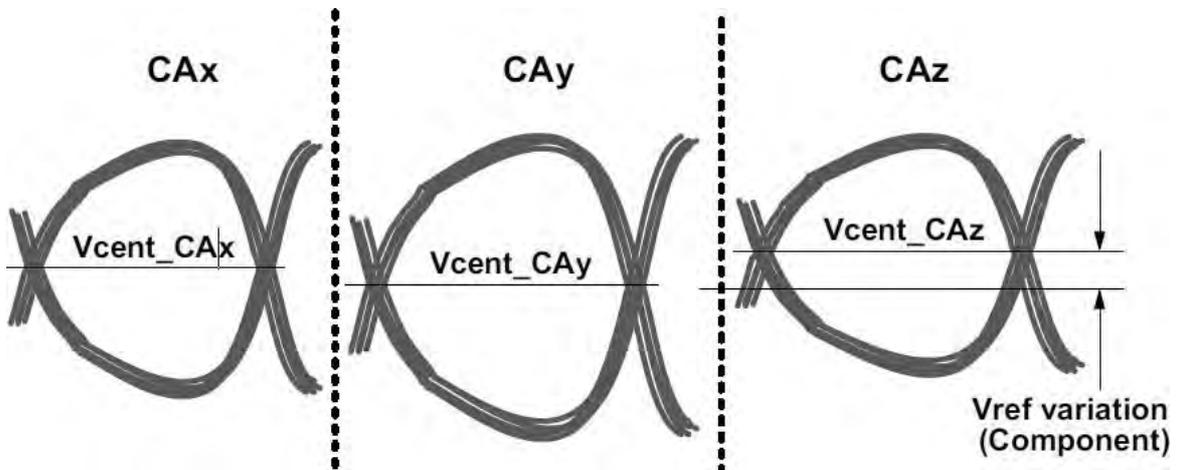


Figure 28. Across pin V_{REFCA} voltage variation

$V_{cent_CA}(\text{pin avg})$ is defined as the midpoint between the largest V_{cent_CA} voltage level and the smallest V_{cent_CA} voltage level across all CA and CS pins for a given DRAM component. Each CA V_{cent} level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 28. This clarifies that any DRAM component level variation must be accounted for within the DRAM CA Rx mask. The component level V_{ref} will be set by the system to account for Ron and ODT settings.

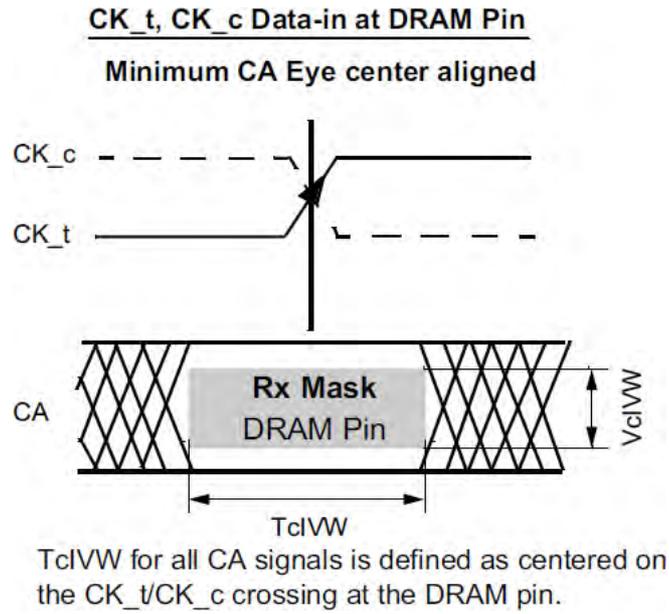


Figure 29. CA Timings at the DRAM pins

All of the timing terms in Figure 29. are measured from the CK_t/CK_c to the center(midpoint) of the TcIVW window taken at the VcIVW_total voltage levels centered around Vcent_CA(pin mid).

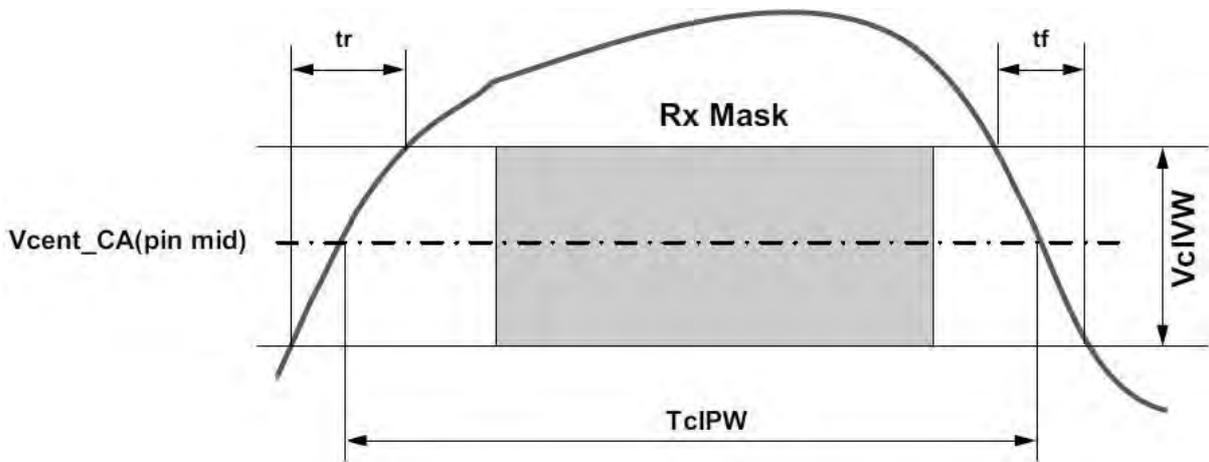


Figure 30. CA TcIPW and SRIN_cIVW definition (for each input pulse)

NOTE :

1) $SRIN_cIVW = VcIVW_Total / (tr \text{ or } tf)$, signal must be monotonic within tr and tf range.

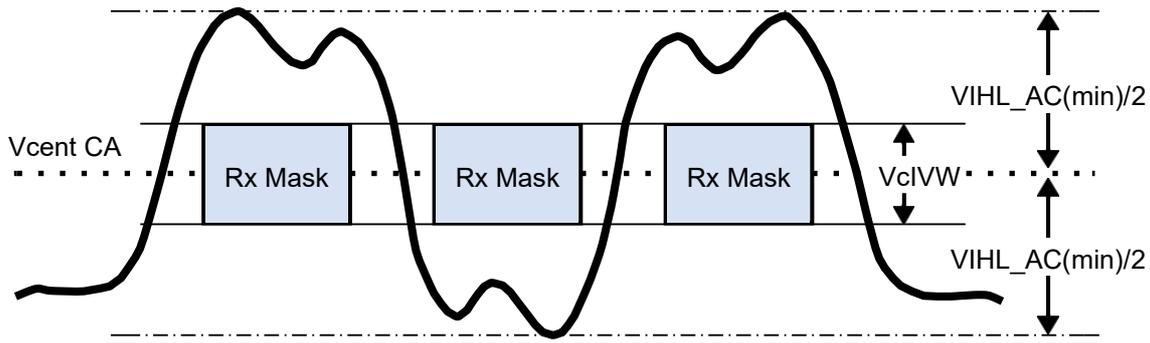


Figure 31. CA VIH_LAC definition (for each input pulse)

[Table 65] DRAM CMD/ADR, CS

| Symbol | Parameter | DQ-1333 ^{A)} | | DQ-1600/1866 | | DQ-3200 | | DQ-3733 | | DQ-4266 | | Unit | NOTE |
|-----------|-----------------------------------|-----------------------|-----|--------------|-----|---------|-----|---------|-----|---------|-----|------|-------|
| | | min | max | min | max | min | max | min | max | min | max | | |
| VcIVW | Rx Mask voltage - p-p | - | 175 | - | 175 | - | 155 | - | 150 | - | 145 | mV | 1,2,3 |
| TcIVW | Rx timing window | - | 0.3 | - | 0.3 | - | 0.3 | - | 0.3 | - | 0.3 | UI* | 1,2,3 |
| VIHL_AC | CA AC input pulse amplitude pk-pk | 210 | - | 210 | - | 190 | - | 180 | - | 180 | - | mV | 4,7 |
| TcIPW | CA input pulse width | 0.55 | - | 0.55 | - | 0.6 | - | 0.6 | - | 0.6 | - | UI* | 5 |
| SRIN_cIVW | Input Slew Rate over VcIVW | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | V/ns | 6 |

* UI=tCK(avg)min

- NOTE :**
- 1) CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
 - 2) Rx mask voltage VcIVW total(max) must be centered around Vcent_CA (pin_mid).
 - 3) Vcent_CA must be within the adjustment range of the CA internal Vref.
 - 4) CA only input pulse signal amplitude into the receiver must meet or exceed VIH_LAC at any point over the total UI. No timing requirement above level. VIH_LAC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIH_LAC/2 min must be met both above and below Vcent_CA.
 - 5) CA only minimum input pulse width defined at the Vcent_CA (pin mid).
 - 6) Input slew rate over VcIVW Mask centered at Vcent_CA (pin mid).
 - 7) VIH_LAC does not have to be met when no transitions are occurring.

A) The following Rx voltage and absolute timing requirements apply for DQ operating frequencies at or below 1333 for all speed bins. For example the TcIVW(ps) = 450ps at or below 1333 operating frequencies.

13.6 DRAM Data Timing

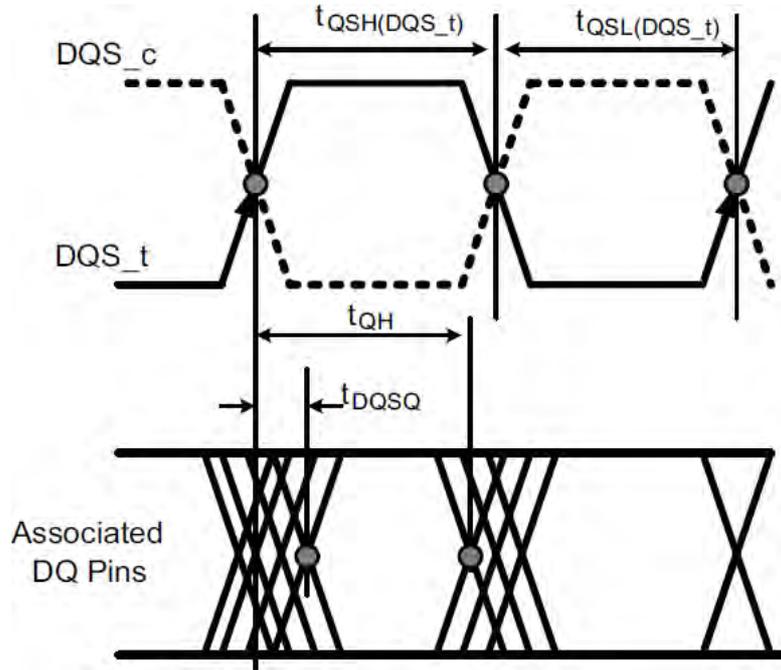


Figure 32. Read data timing definitions t_{QH} and t_{DQSQ} across on DQ signals per DQS group

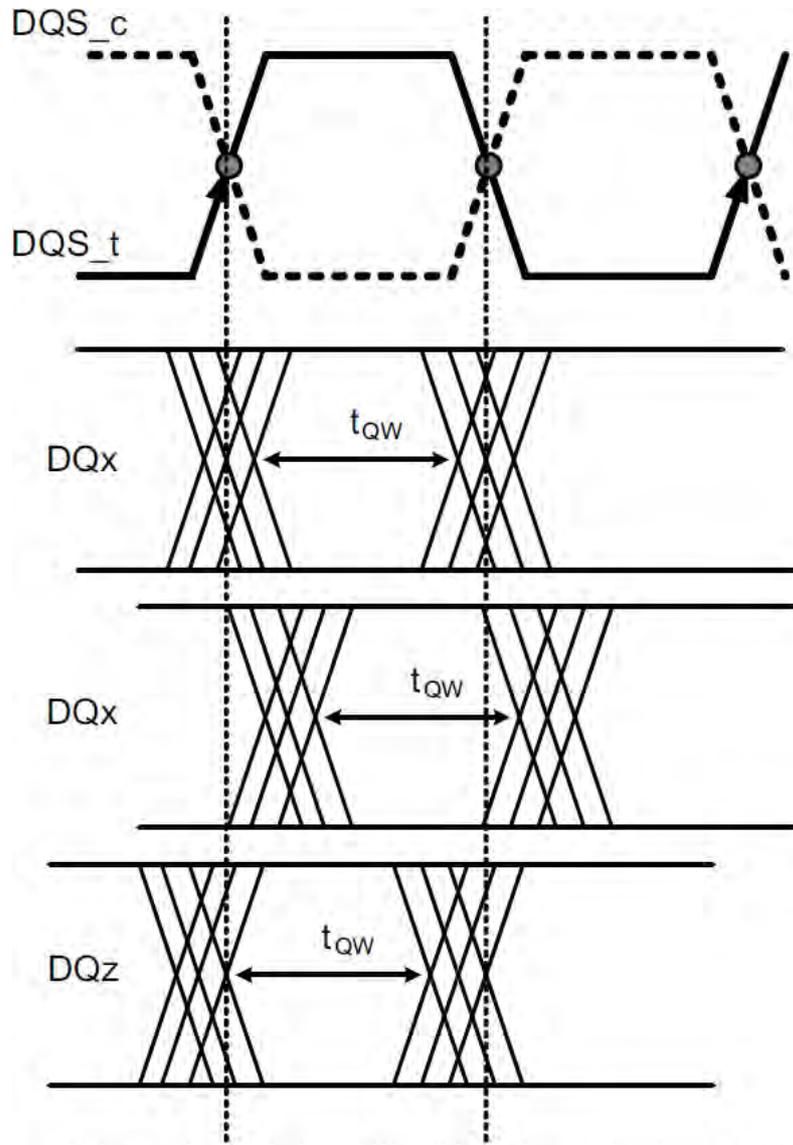


Figure 33. Read data timing t_{QW} valid window defined per DQ signal

[Table 66] Read output timings

| Parameter | Symbol | LPDDR4x-1600/ 1866 | | LPDDR4x-2133/ 2400 | | LPDDR4x-3200 | | LPDDR4x-3733 | | LPDDR4x-4266 | | Units | Notes |
|--|------------------------------------|---|------|---|------|---|------|---|------|---|------|----------------------|-------|
| | | Min | Max | | |
| Data Timing | | | | | | | | | | | | | |
| DQS _t , DQS _c to DQ Skew total, per group, per access (DBI-Disabled) | t _{DQSQ} | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | UI | |
| DQ output hold time total from DQS _t , DQS _c (DBI-Disabled) | t _{QH} | min(t _{QS} _H , t _{QSL}) | - | min(t _{QS} _H , t _{QSL}) | - | min(t _{QS} _H , t _{QSL}) | - | min(t _{QS} _H , t _{QSL}) | - | min(t _{QS} _H , t _{QSL}) | - | UI | |
| DQ output window time total, per pin (DBI-Disabled) | t _{QW_{total}} | 0.75 | - | 0.73 | - | 0.7 | - | 0.7 | - | 0.7 | - | UI | 3 |
| DQ output window time deterministic, per pin (DBI-Disabled) | t _{QW_{dj}} | - | TBD | UI | 2,3 |
| DQS _t , DQS _c to DQ Skew total, per group, per access (DBI-Enabled) | t _{DQSQ_{DBI}} | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | - | 0.18 | UI | |
| DQ output hold time total from DQS _t , DQS _c (DBI-Enabled) | t _{QH_{DBI}} | min(t _{QSH_DBI} , t _{QSL_{DBI}}) | - | min(t _{QSH_DBI} , t _{QSL_{DBI}}) | - | min(t _{QSH_DBI} , t _{QSL_{DBI}}) | - | min(t _{QSH_DBI} , t _{QSL_{DBI}}) | - | min(t _{QSH_DBI} , t _{QSL_{DBI}}) | - | TBD | UI |
| DQ output window time total, per pin (DBI-Enabled) | t _{QW_{total}DBI} | 0.75 | - | 0.73 | - | 0.7 | - | 0.7 | - | 0.7 | - | UI | 3 |
| Data Strobe Timing | | | | | | | | | | | | | |
| DQS _t , DQS _c differential output low time (DBI-Disabled) | t _{QSL} | t _{CL(ABS)} _{0.05} | - | t _{CL(ABS)} _{-0.05} | - | t _{CK(avg)} | 3,4 |
| DQS _t , DQS _c differential output high time (DBI-Disabled) | t _{QSH} | t _{CH(ABS)} _{0.05} | - | t _{CH(ABS)} _{-0.05} | - | t _{CH(ABS)} _{-0.05} | - | t _{CH(ABS)} _{-0.05} | - | t _{CL(ABS)} _{-0.05} | - | t _{CK(avg)} | 3,5 |
| DQS _t , DQS _c differential output low time (DBI-Enabled) | t _{QSL_{DBI}} | t _{CL(ABS)} _{0.045} | - | t _{CL(ABS)} _{-0.045} | - | t _{CK(avg)} | 4,6 |
| DQS _t , DQS _c differential output high time (DBI-Enabled) | t _{QSH_{DBI}} | t _{CH(ABS)} _{0.045} | - | t _{CH(ABS)} _{-0.045} | - | t _{CK(avg)} | 5,6 |

Unit UI = tCK(avg)min/2

- NOTE :**
- 1) The deterministic component of the total timing. Measurement method tbd.
 - 2) This parameter will be characterized and guaranteed by design.
 - 3) This parameter is function of input clock jitter. These values assume the min tCH(ABS) and tCL(ABS). When the input clock jitter min tCH(ABS) and tCL(ABS) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(ABS)-0.04 and tQSH will be tCH(ABS) -0.04.
 - 4) tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
 - 5) tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
 - 6) This parameter is function of input clock jitter. These values assume the min tCH(ABS) and tCL(ABS). When the input clock jitter min tCH(ABS) and tCL(ABS) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(ABS)-0.04 and tQSH will be tCH(ABS) -0.04.

13.7 DQ Rx Voltage And Timing

The DQ input receiver mask for voltage and timing is shown Figure 34. is applied per pin. The “total” mask (V_{dIVW_total} , T_{dIVW_total}) defines the area the input signal must not encroach in order for the DQ input receiver to successfully capture an input signal with a BER of lower than tbd. The mask is a receiver property and it is not the valid data-eye.

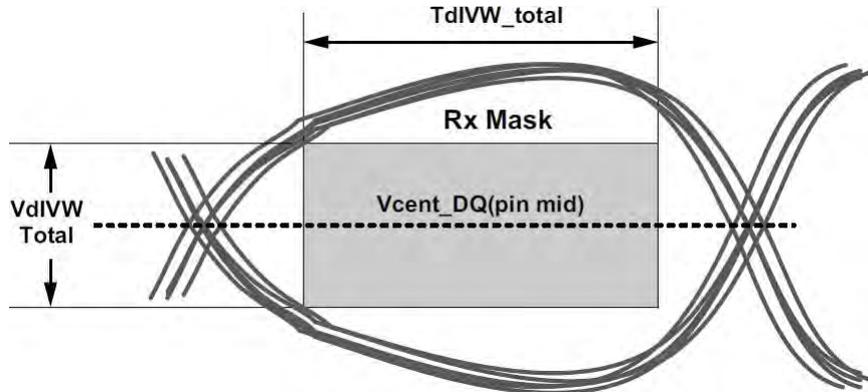


Figure 34. DQ Receiver(Rx) mask

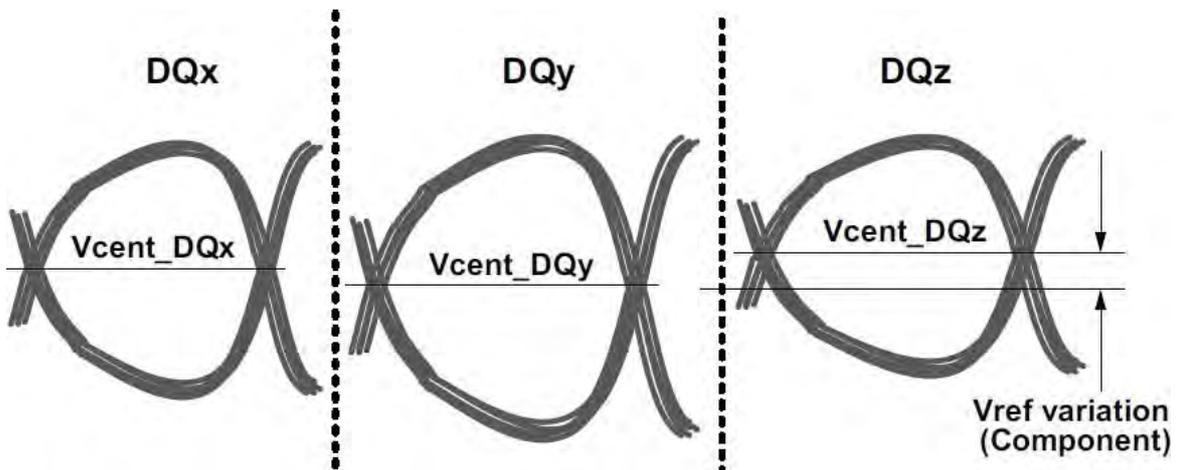


Figure 35. Across pin V_{REFDQ} voltage variation

$V_{cent_DQ(pin\ mid)}$ is defined as the midpoint between the largest V_{cent_DQ} voltage level and the smallest V_{cent_DQ} voltage level across all DQ pins for a given DRAM component. Each DQ V_{cent} is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in Figure 35..This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask. The component level V_{ref} will be set by the system to account for R_{on} and ODT settings.

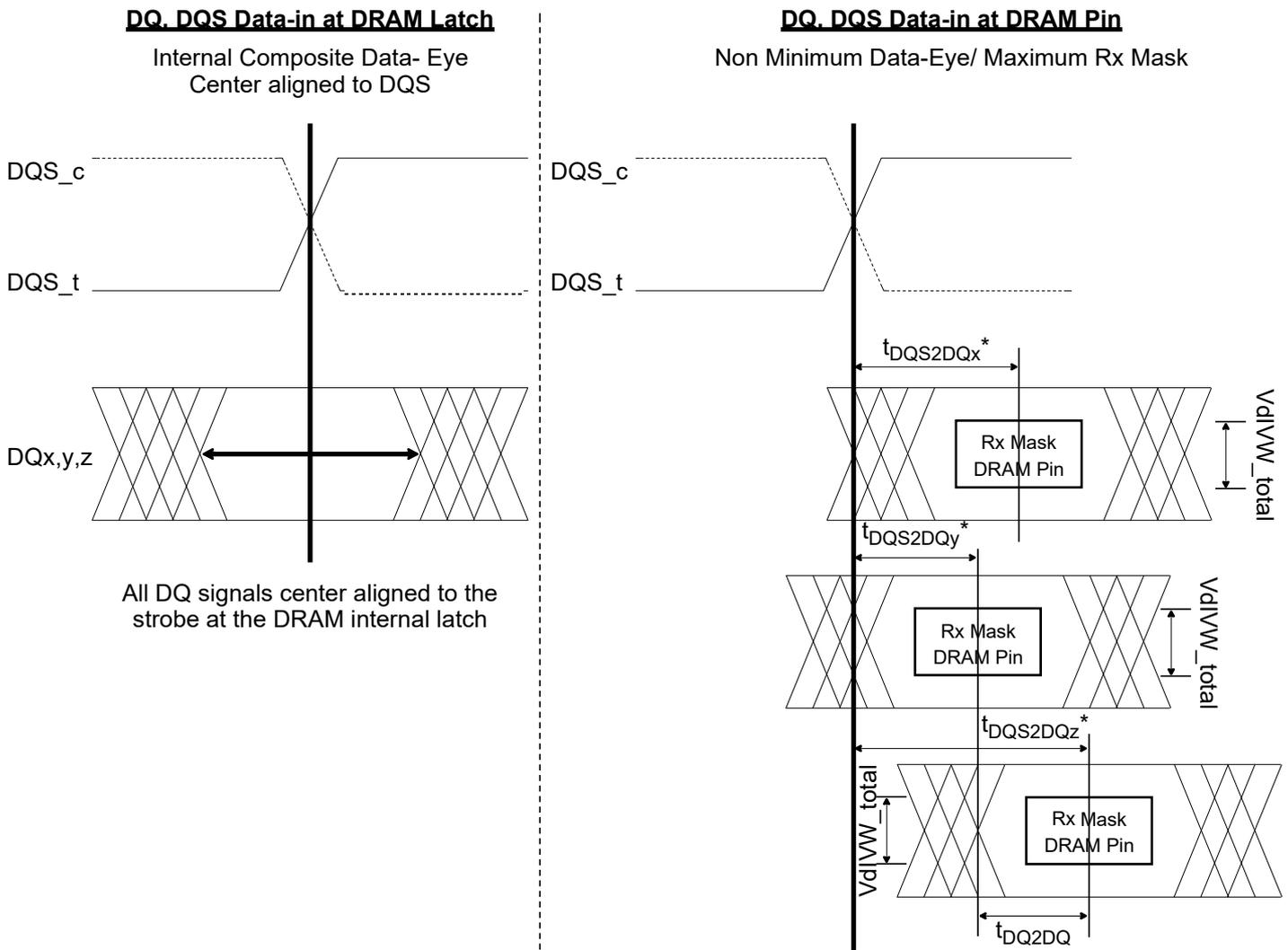


Figure 36. DQ to DQS t_{DQS2DQ} & t_{DQDQ} Timings at the DRAM pins referenced from the internal latch

NOTE :

- 1) t_{DQS2DQ} is measured at the center(midpoint) of the TdiVW window.
- 2) DQz represents the max t_{DQS2DQ} in this example.
- 3) DQy represents the min t_{DQS2DQ} in this example.

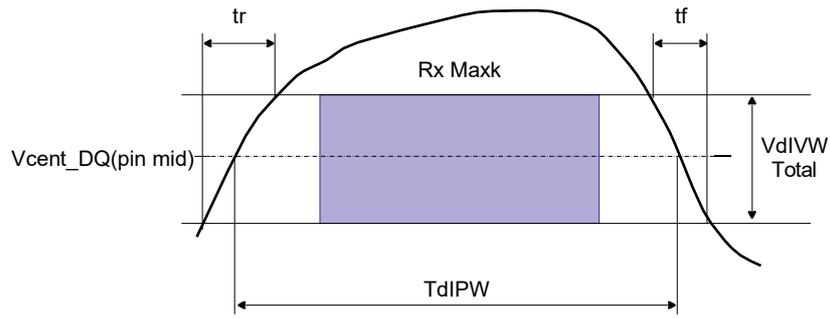


Figure 37. DQ TdIPW and SRIN_dIVW definition (for each input pulse)

NOTE :

1) $SRIN_dIVW = VdIVW_Total / (tr \text{ or } tf)$, signal must be monotonic within tr and tf range.

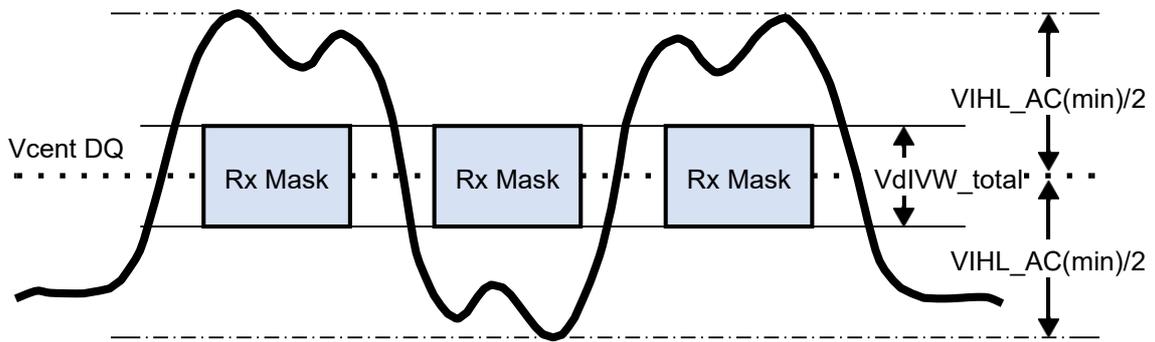


Figure 38. DQ VIH_L_AC definition (for each input pulse)

[Table 67] DRAM DQs In Receive Mode;

| Symbol | Parameter | 1600/1866 ^{A)} | | 2133/2400 | | 3200 | | 3733 | | 4266 | | Unit | NOTE |
|-------------------------------|---|-------------------------|------|-----------|------|------|------|------|------|------|------|---------|----------|
| | | min | max | min | max | min | max | min | max | min | max | | |
| VdIVW_total | Rx Mask voltage - p-p total | - | 140 | - | 140 | - | 140 | - | 130 | - | 120 | mV | 1,2,3,4 |
| TdIVW_total | Rx timing window total (At VdIVW voltage levels) | - | 0.22 | - | 0.22 | - | 0.25 | - | 0.25 | - | 0.25 | UI* | 1,2,4 |
| TdIVW_1bit | Rx timing window 1 bit toggle (At VdIVW voltage levels) | - | TBD | - | TBD | - | TBD | - | TBD | - | TBD | UI* | 1,2,4,12 |
| VIHL_AC | DQ AC input pulse amplitude pk-pk | 180 | - | 180 | - | 180 | - | 180 | - | 170 | - | mV | 5,13 |
| TdIPW DQ | Input pulse width (At Vcent_DQ) | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | 0.45 | - | UI* | 6 |
| t _{DQS2DQ} | DQ to DQS offset | 250 | 700 | 250 | 700 | 250 | 700 | 250 | 700 | 200 | 800 | ps | 7 |
| t _{DQ2DQ} | DQ to DQ offset | - | 30 | - | 30 | - | 30 | - | 30 | - | 30 | ps | 8 |
| t _{DQS2DQ_temp} | DQ to DQS offset temperature variation | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.4 | - | 0.6 | ps/°C | 9 |
| t _{DQS2DQ_volt} | DQ to DQS offset voltage variation | - | 25 | - | 25 | - | 25 | - | 25 | - | 33 | ps/50mV | 10 |
| SRIN_dIVW | Input Slew Rate over VdIVW_total | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | 1 | 7 | V/ns | 11 |
| t _{DQS2DQ_rank2rank} | DQ to DQS offset rank to rank variation | - | 200 | - | 200 | - | 200 | - | 200 | - | 200 | ps | 14,15,16 |

* UI=tck(avg)min/2

NOTE :

- 1) Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
- 2) The design specification is a BER <td. The BER will be characterized and extrapolated if necessary using a dual dirac method.
- 3) Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
- 4) Vcent_DQ must be within the adjustment range of the DQ internal Vref.
- 5) DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ
- 6) DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
- 7) DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation
- 8) DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
- 9) TDQS2DQ max delay variation as a function of temperature.
- 10) TDQS2DQ max delay variation as a function of the DC voltage variation for VDDQ and VDD2. It includes the VDDQ and VDD2 AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package.
- 11) Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
- 12) Rx mask defined for a one pin toggling with other DQ signals in a steady state.
- 13) VIHL_AC does not have to be met when no transitions are occurring.
- 14) The same voltage and temperature are applied to t_{DQS2DQ_rank2rank}.
- 15) t_{DQS2DQ_rank2rank} parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.
- 16) t_{DQS2DQ_rank2rank} support was added to JESD209-4B, some older devices designed to support JESD209-4 and JESD209-4A may not support this parameter. Refer to vendor datasheet.

A) The following Rx voltage and absolute timing requirements apply for all DQ operating frequencies at or below 1600 for all speed bins. For example TdIVW_total(ps) = 137.5ps at or below 1600 operating frequencies.

PART NUMBERING SYSTEM

| LPDDR4X PART NUMBERING SYSTEM | | | | | | | | | |
|--|---|--|---|---|--|----------------------------------|---|--|---|
| AS4C | 512M32 | MD4V | A | - | 62 | B | C/I/A | N | XX |
| AS : Alliance Memory 4C : DRAM Product Line | Memory Organization 512M16: 8Gb (512Mx16) 512M32: 16Gb (512Mx32) 1G32: 32Gb (1Gx32) | Product MD4V : LPDDR4X | Blank : initial release A : Die Rev.A | - | Max Clock 062: 1600MHz 053: 1866MHz 046: 2133MHz | Package B: FBGA | Temperature C: Commercial I : Industrial A: Automotive | N: Lead Free &Halogen Free | Packing Media None: Tray TR : Reel |



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