IS21EF04GP IS22EF04GP

IS21EF08GP IS22EF08GP

4GB/8GB eMMC in pSLC MODE NAND/eMMC 5.1 Interface

DATA SHEET

4GB/8GB eMMC in pSLC Mode NAND/eMMC 5.1 Interface

FEATURES

- Packaged NAND flash memory with *eMMC* 5.1 interface
  - IS21/22EF04GP: 4Gigabyte
  - IS21/22EF08GP: 8Gigabyte
- Device is compliant with *eMMC* Specification Ver.4.3, 4.4, 4.41,4.5, 4.51, 5.0, 5.1
- Bus mode
  - High-speed *eMMC* protocol
  - Clock frequency: 0-200MHz.
  - Ten-wire bus (clock, 1 bit command, 8 bit data bus) and a hardware reset.
- Supports three different data bus widths: 1-bit(default), 4 bits, 8 bits
  - Data transfer rate: up to 52Mbyte/s (using 8 parallel data lines at 52 MHz)
  - Single data rate: up to 200Mbyte/s @ 200MHz (HS200)
  - Dual data rate: up to 400Mbyte/s @ 200MHz (HS400)
- Operating voltage range:
  - VCCQ = 1.8 V/3.3 V
  - VCC = 3.3 V
- Configured as pseudo-SLC (pSLC) mode for higher read/write performance, endurance, and reliability.
- Error free memory access
  - Internal error correction code (ECC) to protect data communication
  - Internal enhanced data management algorithm
  - Solid protection from sudden power failure, safe-update operations for data content
- Security
  - Support secure bad block erase and trim commands
  - Enhanced write protection with permanent and partial protection options
- Major supported features
  - HS400, Field Firmware Update (FFU), Power Off Notification, Pre EOL information, Enhanced Device Life time, Optimal Size.
- Major supported eMMC 5.1 features
  - Enhanced Strobe, Cache Flushing Report, BKOPS Control, Cache Barrier, RPMB Throughput Improve, Secure Write Protection.
- CMD Queuing is not supported.

- Operating Temperature:
  - Industrial Grade: -40 ℃ ~ 85 ℃
  - Automotive Grade (A2): -40 ℃ ~ 105 ℃
- Storage Temperature: -40 ℃ ~ 105 ℃

- Package
  - 153 FBGA (11.5mm x 13mm x 1.0mm)
  - 100 FBGA (14.0mm x 18.0mm x 1.4mm)
  - Green Package (RoHS Compliant, Halogen-Free) and TSCA Compliant

GENERAL DESCRIPTION

ISSI *eMMC* products follow the JEDEC *eMMC* 5.1 standard. It is ideal for embedded storage solutions for Industrial application and automotive application, which require high performance across a wide range of operating temperatures.

eMMC encloses the pSLC Mode NAND and *eMMC* controller inside as one JEDEC standard package, providing a standard interface to the host. The *eMMC* controller directly manages NAND flash, including ECC, wear-leveling, IOPS optimization and read sensing.

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1. PERFORMANCE SUMMARY

1.1 Operating Voltage

Symbol	Min	Max	Unit
V_{CCQ}	1.7/2.7	1.95/3.6	V
V_{CC}	2.7	3.6	V

1.2 Power Consumption

Table 1.1 Dvice Power Consumption (RMS)

Speed Mode & Operation			Industrial Grade		Auto. A2 Grade		Unit
			4GB	8GB	4GB	8GB	
HS400	Read	I_{CC}	45	45	45	45	mA
		I_{CCQ}	175	175	175	175	mA
	Write	I_{CC}	40	75	40	75	mA
		I_{CCQ}	80	85	80	85	mA
HS200	Read	I_{CC}	40	40	40	40	mA
		I_{CCQ}	140	145	140	145	mA
	Write	I_{CC}	40	75	40	75	mA
		I_{CCQ}	80	85	80	85	mA
DDR52	Read	I_{CC}	25	25	25	25	mA
		I_{CCQ}	130	130	130	130	mA
	Write	I_{CC}	40	65	40	65	mA
		I_{CCQ}	70	75	70	75	mA
SDR52	Read	I_{CC}	20	20	20	20	mA
		I_{CCQ}	100	100	100	100	mA
	Write	I_{CC}	40	60	40	60	mA
		I_{CCQ}	70	75	70	75	mA

Notes:

1. The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.
2. The RMS current is measured at T_A=25℃, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width.
3. Current numbers might be subject to changes without notice.

Table 1.2 Device Power Consumption (Standby)

Speed Mode & Operation		Industrial Grade		Auto. A2 Grade		Unit
		4GB	8GB	4GB	8GB	
HS400	Sleep	85	90	85	90	uA
	Standby I_{CCQ}	130	140	130	140	uA
	Standby I_{CC}	40	50	40	50	uA
HS200	Sleep	85	90	85	90	uA
	Standby I_{CCQ}	130	140	130	140	uA
	Standby I_{CC}	40	50	40	50	uA
DDR52	Sleep	90	95	90	95	uA
	Standby I_{CCQ}	140	150	140	150	uA
	Standby I_{CC}	40	55	40	55	uA
SDR52	Sleep	90	95	90	95	uA
	Standby I_{CCQ}	140	150	140	150	uA
	Standby I_{CC}	40	55	40	55	uA

Notes:

1. Standby current is measured at T_A=25℃, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width without clock frequency.
2. Current numbers might be subject to changes without notice.

1.3 Typical Sequential Performance

Table 1.3 Sequential Burst Performance (PSA Pseudo-SLC Burst Status)

Speed Mode & Operation			Industrial Grade		Auto. A2 Grade		Unit
			4GB	8GB	4GB	8GB	
HS400	Write Cache on	Read	225	225	225	225	MB/s
		Write	105	140	105	140	MB/s
	Write Cache off	Read	225	225	225	225	MB/s
		Write	100	125	100	125	MB/s
HS200	Write Cache on	Read	160	160	160	160	MB/s
		Write	105	125	105	125	MB/s
	Write Cache off	Read	160	160	160	160	MB/s
		Write	95	115	95	115	MB/s
DDR52	Write Cache on	Read	80	80	80	80	MB/s
		Write	65	70	65	70	MB/s
	Write Cache off	Read	80	80	80	80	MB/s
		Write	65	65	65	65	MB/s
SDR52	Write Cache on	Read	45	45	45	45	MB/s
		Write	40	40	40	40	MB/s
	Write Cache off	Read	45	45	45	45	MB/s
		Write	35	40	35	40	MB/s

Notes:

1. Values given for an 8-bit bus width, running from ISSI proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 64KB.

Table 1.4 Sequential Sustained Performance (Normal Status)

Speed Mode & Operation			Industrial Grade		Auto. A2 Grade		Unit
			4GB	8GB	4GB	8GB	
HS400	Write Cache on	Read	225	225	225	225	MB/s
		Write	30	60	30	60	MB/s
	Write Cache off	Read	225	225	225	225	MB/s
		Write	20	25	20	25	MB/s
HS200	Write Cache on	Read	160	160	160	160	MB/s
		Write	30	60	30	60	MB/s
	Write Cache off	Read	160	160	160	160	MB/s
		Write	20	25	20	25	MB/s
DDR52	Write Cache on	Read	80	80	80	80	MB/s
		Write	30	55	30	55	MB/s
	Write Cache off	Read	80	80	80	80	MB/s
		Write	20	25	20	25	MB/s
SDR52	Write Cache on	Read	45	45	45	45	MB/s
		Write	30	40	30	40	MB/s
	Write Cache off	Read	45	45	45	45	MB/s
		Write	20	20	20	20	MB/s

Notes:

1. Values given for an 8-bit bus width, running from ISSI proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 64KB.

1.4 Typical Random Performance

Table 1.5 Random Burst Performance (PSA Pseudo-SLC Burst Status)

Speed Mode & Operation			Industrial Grade		Auto. A2 Grade		Unit
			4GB	8GB	4GB	8GB	
HS400	Write Cache on	Read	5200	5300	5200	5300	IOPS
		Write	9800	10200	9800	10200	IOPS
	Write Cache off	Read	2200	2200	2200	2200	IOPS
		Write	1300	1400	1300	1400	IOPS
HS200	Write Cache on	Read	5300	5300	5300	5300	IOPS
		Write	9700	10100	9700	10100	IOPS
	Write Cache off	Read	5300	5300	5300	5300	IOPS
		Write	2200	2200	2200	2200	IOPS
DDR52	Write Cache on	Read	4900	4800	4900	4800	IOPS
		Write	7100	7900	7100	7900	IOPS
	Write Cache off	Read	4900	4900	4900	4900	IOPS
		Write	2200	2100	2200	2100	IOPS
SDR52	Write Cache on	Read	4100	4000	4100	4000	IOPS
		Write	6100	6200	6100	6200	IOPS
	Write Cache off	Read	4100	4100	4100	4100	IOPS
		Write	2000	2000	2000	2000	IOPS

Notes:

1. Values given for an 8-bit bus width, running from ISSI proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 64KB.

Table 1.5 Random Sustained Performance (Normal Status)

Speed Mode & Operation			Industrial Grade		Auto. A2 Grade		Unit
			4GB	8GB	4GB	8GB	
HS400	Write Cache on	Read	4900	4900	4900	4900	IOPS
		Write	6400	6400	6400	6400	IOPS
	Write Cache off	Read	4900	4900	4900	4900	IOPS
		Write	1500	1400	1500	1400	IOPS
HS200	Write Cache on	Read	4900	5000	4900	5000	IOPS
		Write	6200	6300	6200	6300	IOPS
	Write Cache off	Read	4900	5000	4900	5000	IOPS
		Write	1400	1400	1400	1400	IOPS
DDR52	Write Cache on	Read	4500	4600	4500	4600	IOPS
		Write	5800	5900	5800	5900	IOPS
	Write Cache off	Read	4500	4600	4500	4600	IOPS
		Write	1400	1400	1400	1400	IOPS
SDR52	Write Cache on	Read	3900	3900	3900	3900	IOPS
		Write	5200	5400	5200	5400	IOPS
	Write Cache off	Read	3800	3900	3800	3900	IOPS
		Write	1300	1300	1300	1300	IOPS

Notes:

1. Values given for an 8-bit bus width, running from ISSI proprietary tool.
2. Performance is measured at V_{CC}=3.3V, V_{CCQ}=1.8V in HS400 & HS200 mode and at V_{CC}=3.3V, V_{CCQ}=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. The write cache size is 64KB.

1.5 Boot Partition and RPMB (Reply Protected Memory Block)

Table 1.6 Boot Partition and RPMB

Option	Boot Partition 1	Boot Partition 2	RPMB
J	4,096 KB	4,096 KB	4,096 KB
B	16,384 KB	16,384 KB	4,096 KB

1.6 User Density Size

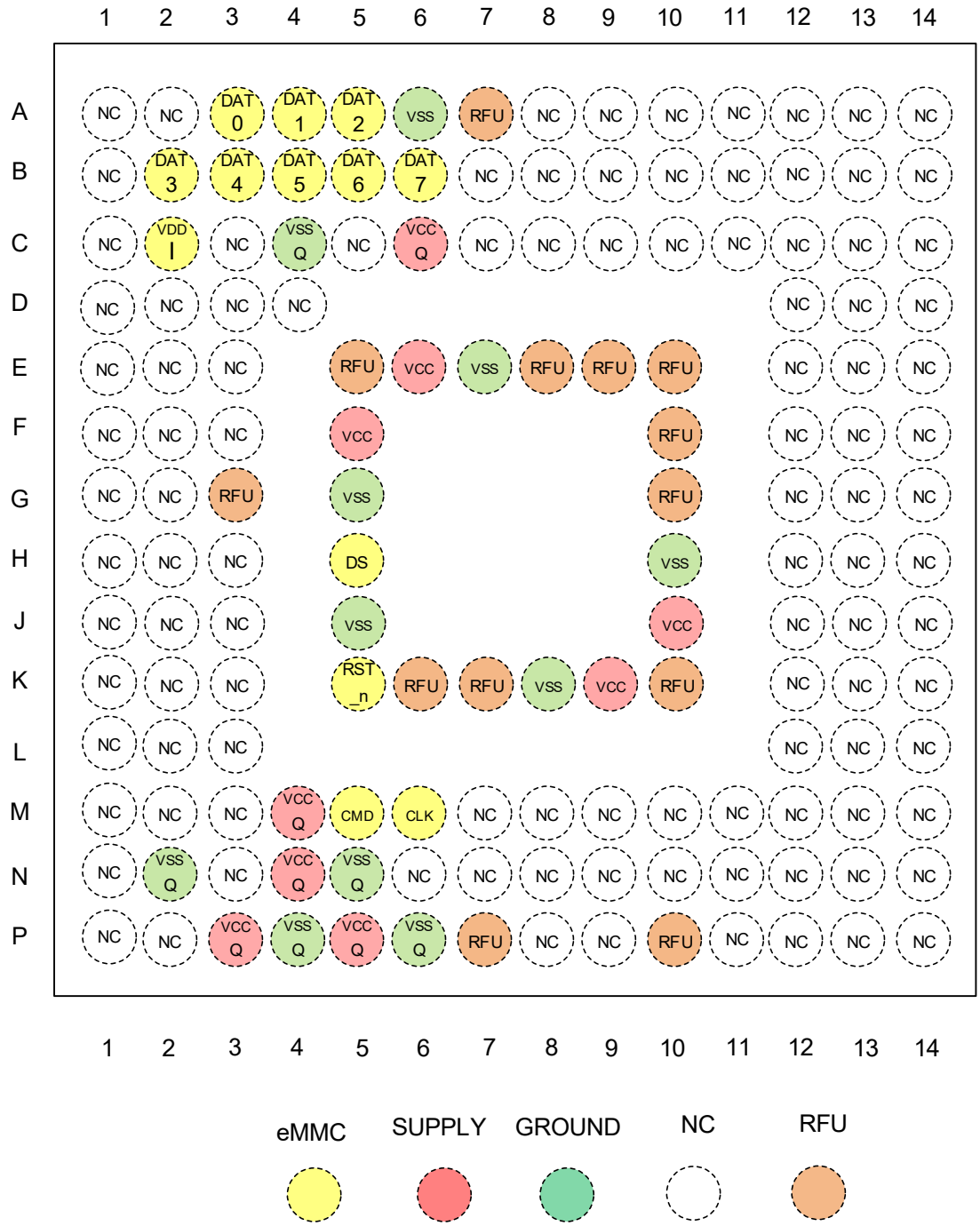
Total user density depends on device type.

Table 1.7 User Density Size

Device	Flash Mode	Option	User Density Size
4GB	pSLC	J	3,917,479,936 Bytes
		B	3,858,759,680 Bytes
8GB	pSLC	J	7,834,959,872 Bytes
		B	7,784,628,224 Bytes

2. PIN CONFIGURATION

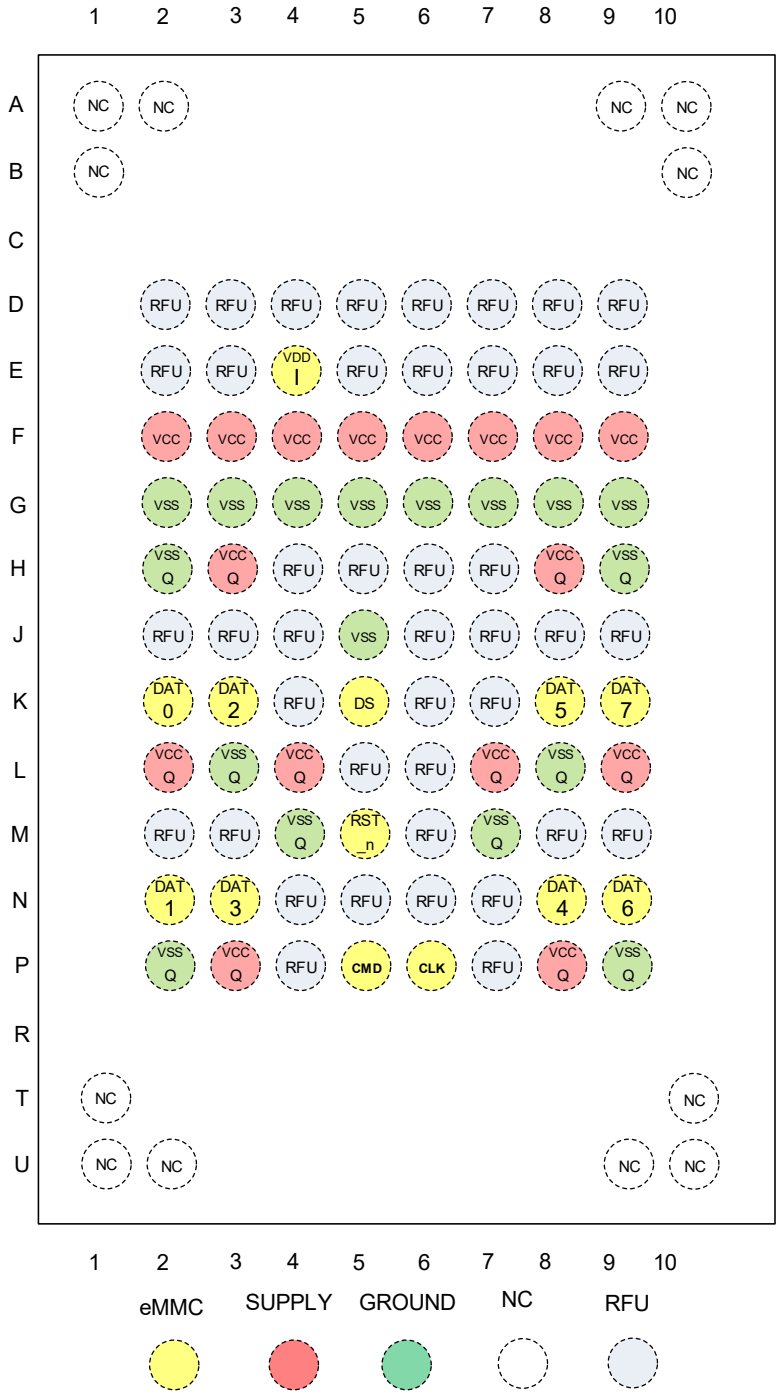
153 FBGA Top View (Ball Down)



Note:

1. H5 (DS), A6 (VSS) and J5 (VSS) can be left floating if HS400 mode is not used.

100 FBGA Top View (Ball Down)



Note:

1. K5 (DS) and J5 (VSS) can be left floating if HS400 mode is not used.

3. PIN DESCRIPTIONS

Pin Name	Type[1]	Pin Function
CLK	I	**DATA INPUT** Each cycle of this signal directs a one bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency
DAT0~DAT7	I/O/PP	**DATA** These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the *eMMC* host controller. The *eMMC* Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.
CMD	I/O/PP/OD	**COMMAND/RESPONSE** This signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the *eMMC* host controller to the *eMMC* Device and responses are sent from the Device to the.host.
RST#	I	**HARDWARE RESET**
DS	O/PP	**Data Strobe** This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.
VDDI		**INTERNAL VOLTAGE NODE** At least a 0.1uF capacitor is required to connect VDDI to ground. A 1uF capacitor is recommended. Do not tie to supply voltage or ground.
VCC	-	**POWER SUPPLY** VCC is the power supply for Core
VCCQ	-	**POWER SUPPLY** VCC is the power supply for I/O
VSS	-	**Ground** VSS is the ground for Core
VSSQ	-	**GROUND** VSSQ is the ground for I/O
RFU		**Reserved For Future Use**
N.C.		**NO CONNECTION** Lead is not internally connected.

Note:

1. I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power

4. eMMC Device and System

4.1 eMMC System Overview

The eMMC specification covers the behavior of the interface and the device controller. As part of this specification the existence of a host controller and a memory storage array are implied but the operation of these pieces is not fully specified.

The Device consists of a single chip MMC controller and NAND flash memory module. The micro-controller interfaces with a host system allowing data to be written to and read from the NAND flash memory module. The controller allows the host to be independent from details of erasing and programming the flash memory

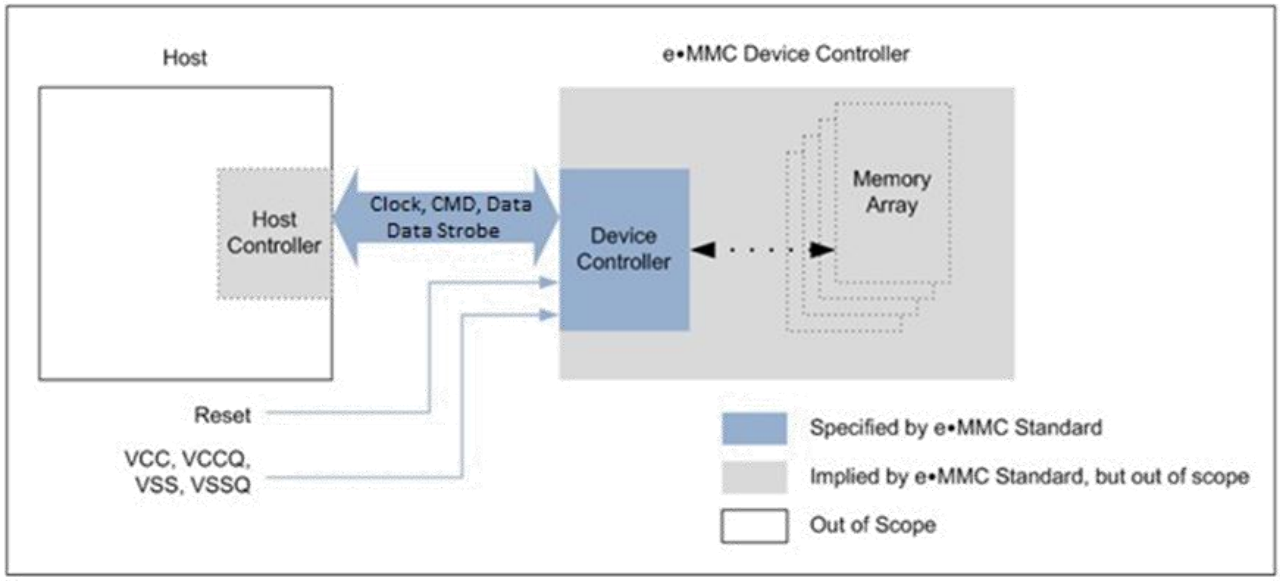


Figure 4.1 eMMC System Overview

4.2 Memory Addressing

The Previous implementations of the eMMC specification are following byte addressing with 32-bit field. This addressing mechanism permitted for eMMC densities up to and including 2 GB.

To support larger density, the addressing mechanism was update to support sector addresses (512 B sectors). The sector addresses shall be used for all devices with capacity larger than 2 GB.

To determine the addressing mode, use the host should read bit [30:29] in the OCR register. specified.

4.3 eMMC Device Overview

The eMMC device transfers data via a configurable number of data bus signals. The communication signals are:

1.3.1 Clock (CLK)

Each cycle of this signal directs a one-bit transfer on the command and either a one bit (1x) or a two bits transfer (2x) on all the data lines. The frequency may vary between zero and the maximum clock frequency

1.3.2 Data Strobe

Each This signal is generated by the device and used for output in HS400 mode. The frequency of this signal follows the frequency of CLK. For data output each cycle of this signal directs two bits transfer(2x) on the data - one bit for positive edge and the other bit for negative edge. For CRC status response output and CMD response output (enabled only HS400 enhanced strobe mode), the CRC status is latched on the positive edge only, and don't care on the negative edge.

1.3.3 Command (CMD)

Each his signal is a bidirectional command channel used for Device initialization and transfer of commands. The CMD signal has two operation modes: open-drain for initialization mode, and push-pull for fast command transfer. Commands are sent from the eMMC host controller to the eMMC Device and responses are sent from the Device to the host.

1.3.4 Input/Outputs (DAT0-DAT7)

These are bidirectional data channels. The DAT signals operate in push-pull mode. Only the Device or the host is driving these signals at a time. By default, after power up or reset, only DAT0 is used for data transfer. A wider data bus can be configured for data transfer, using either DAT0-DAT3 or DAT0-DAT7, by the eMMC host controller. The eMMC Device includes internal pull-ups for data lines DAT1-DAT7. Immediately after entering the 4-bit mode, the Device disconnects the internal pull ups of lines DAT1, DAT2, and DAT3. Correspondingly, immediately after entering to the 8-bit mode the Device disconnects the internal pull-ups of lines DAT1–DAT7.

Table 4.1 Communication Interface

Name	Type[1]	Description
CLK	I	Clock
DAT0	I/O/PP	Data
DAT1	I/O/PP	Data
DAT2	I/O/PP	Data
DAT3	I/O/PP	Data
DAT4	I/O/PP	Data
DAT5	I/O/PP	Data
DAT6	I/O/PP	Data
DAT7	I/O/PP	Data
CMD	I/O/PP/OD	Command/Response
RST_n	I	Hardware reset
VCC	S	Supply voltage for Core
VCCQ	S	Supply voltage for I/O
VSS	S	Supply voltage ground for Core
VSSQ	S	Supply voltage ground for I/O
DS	O/PP	Data strobe
VDDi		Connect capacitor from VDDi to GND for stabilize internal power.

Note:

1. I: input; O: output; PP: push-pull; OD: open-drain; NC: Not connected (or logical high); S: power supply.

4.4 eMMC BUS

The *eMMC* bus has ten communication lines and three supply lines:

- CMD： Command is a bidirectional signal. The host and Device drivers are operating in two modes, open drain and push/pull.
- DAT0-7： Data lines are bidirectional signals. Host and Device drivers are operating in push-pull mode
- CLK： Clock is a host to Device signal. CLK operates in push-pull mode
- Data Strobe: Data Strobe is a Device to host signal. Data Strobe operates in push-pull mode.

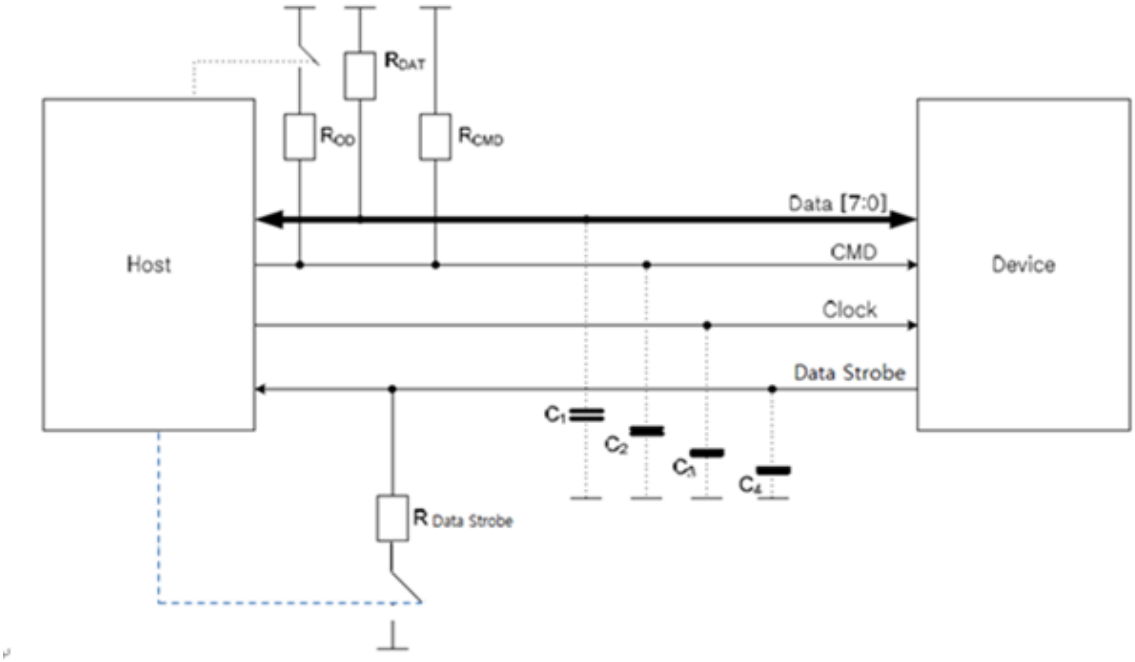


Figure 4.2 BUS Circuitry Diagram

The R_{OD} is switched on and off by the host synchronously to the open-drain and push-pull mode transitions. The host does not have to have open drain drivers, but must recognize this mode to switch on the R_{OD}. R_{DAT} and R_{CMD} are pull-up resistors protecting the CMD and the DAT lines against bus floating device when all device drivers are in a high-impedance mode.

A constant current source can replace the R_{OD} by achieving a better performance (constant slopes for the signal rising and falling edges). If the host does not allow the switchable R_{OD} implementation, a fixed R_{CMD} can be used).Consequently the maximum operating frequency in the open drain mode has to be reduced if the used R_{CMD} value is higher than the minimal one given in.
$R_{Data\ strobe}$ is pull-down resistor used in HS400 device.

5. REGISTER SETTINGS

Within the Device interface six registers are defined: OCR, CID, CSD, EXT_CSD, RCA and DSR. These can be accessed only by corresponding commands (see Section 6.10 of JESD84-B51).

5.1 OCR Register

The 32-bit operation conditions register (OCR) stores the VDD voltage profile of the Device and the access mode indication. In addition, this register includes a status information bit. This status bit is set if the Device power up procedure has been finished. The OCR register shall be implemented by all Devices.

Table 5.1 OCR Register

VCCQ Voltage Window	Width (Bits)	OCR Bit	OCR Value
Device power up status bit (busy) (1)	1	[31]	Note 1
Access Mode	2	[30:29]	10b (sector mode)
Reserved	5	[28:24]	0 0000b
VCCQ: 2.7 – 3.6V	9	[23:15]	1 1111 1111b
VCCQ: 2.0 – 2.6V	7	[14:8]	000 0000b
VCCQ: 1.7 – 1.95V	1	[7]	1b
Reserved	7	[6:0]	000 0000b

Note:

1. This bit is set to LOW if the device has not finished the power up routine.

5.2 CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase (*eMMC* protocol).

Table 5.2 CID Register

CID Fields Name		Field	Width	CID slice	Value
Manufacturer ID		MID	8	[127:120]	9Dh
Reserved		-	6	[119:114]	-
Device/BGA		CBX	2	[113:112]	1h
OEM/Application ID		OID	8	[111:104]	1h
Product name	4GB	PNM	48	[103:56]	IS004G
	8GB				IS008G
Product revision		PRV	8	[55:48]	51h*
Product serial number		PSN	32	[47:16]	Random by Production
Manufacturing date		MDT	8	[15:8]	Month, Year
CRC7 checksum		CRC	7	[7:1]	- (1)
Reserved		-	1	[0:0]	1h

Note:

1. The description is same as *e.MMC* ™ JEDEC standard.

CSD Register

The Card-Specific Data (CSD) register provides information on how to access the contents stored in *eMMC*. The CSD registers are used to define the error correction type, maximum data access time, data transfer speed, data format…etc. For details, refer to section 7.3 of the JEDEC Standard Specification No.JESD84-B51.

Table 5.3 CSD Register

Name	Field	Width (Bits)	CSD Bits	CSD Value(1)
CSD Structure	CSD_STRUCTURE	2	[127:126]	3h
System Specification Version	SPEC_VERS	4	[125:122]	4h
Reserved (2)	-	2	[121:120]	-
Data Read Access Time 1	TAAC	8	[119:112]	7Fh
Data Read Access Time 2 in CLK Cycles (NSAC x 100)	NSAC	8	[111:104]	1h
Maximum Bus Clock Frequency	TRAN_SPEED	8	[103:96]	32h
Card Command Classes	CCC	12	[95:84]	8F5h
Maximum Read Data Block Length	READ_BL_LEN	4	[83:80]	9h
Partial Blocks for Reads supported	READ_BL_PARTIAL	1	[79]	0h
Write Block Misalignment	WRITE_BLK_MISALIGN	1	[78]	0h
Read Block Misalignment	READ_BLK_MISALIGN	1	[77]	0h
DS Register Implemented	DSR_IMP	1	[76]	0h
Reserved (2)	-	2	[75:74]	0h
Device Size	C-SIZE	12	[73:62]	FFFh
Maximum Read Current at VDD min	VDD_R_CURR_MIN	3	[61:59]	7h
Maximum Read Current at VDD max	VDD_R_CURR_MAX	3	[58:56]	7h
Maximum Write Current at VDD min	VDD_W_CURR_MIN	3	[55:53]	7h
Maximum Write Current at VDD max	VDD_W_CURR_MAX	3	[52:50]	7h
Device Size Multiplier	C_SIZE_MULT	3	[49:47]	7h
Erase Group Size	ERASE_GRP_SIZE	5	[42:46]	4G-0Fh 8G-1Fh
Erase Group Size Multiplier	ERASE_GRP_SIZE_MULT	5	[41:37]	1Fh
Write Protect Group Size	WR_GRP_SIZE	5	[36:32]	0Fh
Write Protect Group Enable	WR_GRP_ENABLE	1	[31]	1h
Manufacturer Default ECC	DEFAULT_ECC	2	[30:29]	0h
Write-Speed Factor	R2W_FACTOR	3	[28:26]	2h

Name	Field	Width (Bits)	CSD Bits	CSD Value[1]
Maximum Write Data Block Length	WRITE_BL_LEN	4	[25:22]	9h
Partial Blocks for Writes supported	WRITE_BL_PARTIAL	1	[21]	0h
Reserved [2]	-	4	[20:17]	0h
Content Protection Application	CONTENT_PROT_APP	1	[16]	0h
File-Format Group	FILE_FORMAT_GRP	1	[15]	0h
Copy Flag (OTP)	COPY	1	[14]	0h
Permanent Write Protection	PERM_WRITE_PROTECT	1	[13]	0h
Temporary Write Protection	TEMP_WRITE_PROTECT	1	[12]	0h
File Format	FILE_FORMAT	2	[11:10]	0h
ECC	ECC	2	[9:8]	0h
CRC	CRC	7	[7:1]	4G-5Dh 8G-17h
Not Used, always “1”	-	1	[0]	1h

Note:

1. CSD value might be subject to change without notice.

5.3 Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command.

Table 5.4 ECSD Register

Name	Field	Size (Bytes)	ECSD Bits	ECSD Value
Reserved	-	6	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI Features	HPI_FEATURES	1	[503]	1h
Background Operations Support	BKOPS_SUPPORT	1	[502]	1h
Max Packed Read Commands	MAX_PACKED_READS	1	[501]	3Ch
Max Packed Write Commands	MAX_PACKED_WRITES	1	[500]	3Ch
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	3h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context Management Capabilities	CONTEXT_CAPABILITIES	1	[496]	5h
Large Unit Size	LARGE_UNIT_SIZE_M1	1	[495]	17h
Extended Partitions Attribute Support	EXT_SUPPORT	1	[494]	3h
Supported Modes	SUPPORT_MODES	1	[493]	1h
FFU Features	FFU_FEATURES	1	[492]	0h
Operations Code Timeout	OPERATION_CODE_TIEMOUT	1	[491]	0h
FFU Argument	FFU_ARG	4	[490:487]	65535h
Reserved	-	181	[486:306]	1h
Number of FW Sectors Correctly Programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_pROGRAMMED	4	[305:302]	–
Vendor Proprietary Health Report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	[301:270]	0h
Device Life Time Estimation Type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	0h
Device Life Time Estimation Type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	0h
Pre EOL Information	PRE_EOL_INFO	1	[267]	0h

Name	Field		Size (Bytes)	ECSD Bits	ECSD Value(1)
Optimal Read Size	OPTIMAL_READ_SIZE		1	[266]	1h
Optimal Write Size	OPTIMAL_WRITE_SIZE		1	[265]	8h
Optimal Trim Unit Size	OPTIMAL_TRIM_UNIT_SIZE		1	[264]	1h
Device Version	DEVICE_VERSION		2	[263:262]	0
Firmware Version	FIRMWARE_VERSION		8	[261:254]	-
Power Class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360		1	[253]	0h
Cache Size	CACHE_SIZE		4	[252:249]	512
Generic CMD6 Timeout	GENERIC_CMD6_TIME		1	[248]	32h
Power Off Notification (Long) Timeout	POWER_OFF_LONG_TIME		1	[247]	FFh
Background Operations Status	BKOPS_STATUS		1	[246]	0h
Number of Correctly Programmed Sectors	CORRECTLY_PRG_SECTORS_NUM		4	[245:242]	0h
First Initialization Time After Partitioning (First CMD1 to Device ready)	INI_TIMEOUT_PA		1	[241]	64h
Reserved	-		1	[240]	1h
Power Class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360		1	[239]	0h
Power Class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195		1	[238]	0h
Power Class for 200MHz at 3.6V	PWR_CL_200_360		1	[237]	0h
Power Class for 200MHz at 1.95V	PWR_CL_200_195			[236]	0h
Minimum Write Performance for 8-bit at 52MHz in DDR Mode	MIN_PERF_DDR_W_8_52		1	[235]	0h
Minimum Read Performance for 8-bit at 52MHz in DDR Mode	MIN_PERF_DDR_R_8_52		1	[234]	0h
Reserved	-		1	[233]	0h
TRIM Multiplier	TRIM_MULT		1	[232]	11h
Secure Feature Support	SEC_FEATURE_SUPPORT		1	[231]	55h
SECURE ERASE Multiplier	SEC_ERASE_MULT		1	[230]	F7h
SECURE TRIM Multiplier	SEC_TRIM_MULT		1	[229]	F7h
Boot Information	BOOT_INFO		1	[228]	7h
Reserved	-		1	[227]	0h
Boot Partition Size	BOOT_SIZE_MULT	J-Option	1	[226]	20h
		B-Option			80h

Name	Field			Size (Bytes)	ECSD Bits	ECSD Value[1]
Access Size	ACC_SIZE			1	[225]	7h-4GB 8h-8GB
High-Capacity Erase Unit Size	HC_ERASE_GRP_SIZE			1	[224]	1h
High-Capacity Erase Timeout	ERASE_TIMEOUT_MULT			1	[223]	11h
Reliable Write-Sector Count	REL_WR_SEC_C			1	[222]	1h
High-Capacity Write Protect Group Size	HC_WP_GRP_SIZE			1	[221]	10h
Sleep Current (V_{CC})	S_C_VCC			1	[220]	Ah
Sleep Current (V_{CCQ})	S_C_VCCQ			1	[219]	Bh
Production State Awareness Timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT			1	[218]	14h
Sleep/Awake Timeout	S_A_TIMEOUT			1	[217]	15h
Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME			1	[216]	0h
Sector Count	SEC_COUNT	4GB	J-Option	4	[215:212]	7651328[5]
			B-Option			7536440[5]
		8GB	J-Option			15302656[5]
			B-Option			15204352[5]
Reserved	-			1	[211]	1h
Minimum Write Performance for 8-bit at 52MHz	MIN_PERF_W_8_52			1	[210]	8h
Minimum Read Performance for 8-bit at 52MHz	MIN_PERF_R_8_52			1	[209]	8h
Minimum Write Performance for 8-bit at 26MHz and 4-bit at 52MHz	MIN_PERF_W_8_26_4_52			1	[208]	8h
Minimum Read Performance for 8-bit at 26MHz and 4-bit at 52MHz	MIN_PERF_R_8_26_4_52			1	[207]	8h
Minimum Write Performance for 4-bit at 26MHz	MIN_PERF_W_4_26			1	[206]	8h
Minimum Read Performance for 4-bit at 26MHz	MIN_PERF_R_4_26			1	[205]	8h
Reserved	-			1	[204]	0h
Power Class for 26MHz at 3.6V	PWR_CL_26_360			1	[203]	0h
Power Class for 52MHz at 3.6V	PWR_CL_52_360			1	[202]	0h
Power Class for 26MHz at 1.95V	PWR_CL_26_195			1	[201]	0h
Power Class for 52MHz at 1.95V	PWR_CL_52_195			1	[200]	0h
Partition Switching Timing	PARTITION_SWITCH_TIME			1	[199]	3h
Out-of-Interrupt Busy Timing	OUT_OF_INTERRUPT_TIME			1	[198]	FFh

Name	Field	Size (Bytes)	ECSD Bits	ECSD Value(1)
I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Card Type	CARD_TYPE	1	[196]	57h
Reserved	-	1	[195]	0h
CSD Structure Version	CSD_STRUCTURE	1	[194]	2h
Reserved	-	1	[193]	0h
Extended CSD Structure Revision	EXT_CSD_REV	1	[192]	8h
Command Set	CMD_SET	1	[191]	0h
Reserved	-	1	[190]	0h
Command Set Revision	CMD_SET_REV	1	[189]	0h
Reserved	-	1	[188]	0h
Power Class	POWER_CLASS	1	[187]	0h
Reserved	-	1	[186]	0h
High-Speed Interface Timing	HS_TIMING	1	[185]	1h (3)
Reserved	-	1	[184]	1h
Bus Width Mode	BUS_WIDTH	1	[183]	2h (4)
Reserved	-	1	[182]	0h
Erased memory Content	ERASED_MEM_CONT	1	[181]	0h
Reserved	-	1	[180]	0h
Partition Configuration	PARTITION_CONFIG	1	[179]	0h
Boot Configuration Protection	BOOT_CONFIG_PROT	1	[178]	0h
Boot Bus Width	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved	-	1	[176]	0h
High-Density Erase Group Definition	ERASE_GROUP_DEF	1	[175]	0h
Boot Write Protection Status Registers	BOOT_WP_STATUS	1	[174]	0h
Boot Area Write Protection Register	BOOT_WP	1	[173]	0h
Reserved	-	1	[172]	0h
User Write Protection Register	USER_WP	1	[171]	0h
Reserved	-	1	[170]	0h
Firmware Configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write Reliability Setting Register	WR_REL_SET	1	[167]	1Fh
Write Reliability Parameter Register	WR_REL_PARAM	1	[166]	14h
Start Sanitize Operation	SANITIZE_START	1	[165]	0h
Manually Start Background Operations	BKOPS_START	1	[164]	0h

Name	Field			Size (Bytes)	ECSD Bits	ECSD Value(1)
Enable Background Operations Handshake	BKOPS_EN			1	[163]	0h
Hardware Reset Function	RST_n_FUNCTION			1	[162]	0h
HPI Management	HPI_MGMT			1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT			1	[160]	7h
Maximum Enhanced Area Size	MAX_ENH_SIZE_MULT	4GB	J-Option	3	[159:157]	467h
			B-Option			460h
		8GB	J-Option			934h
			B-Option			928h
Partitions Attribute	PATTITIONS_ATTRIBUTE			1	[156]	1h
Partitioning Setting	PARTITIONING_SETTING_COMPLETED			1	[155]	1h
General-Purpose Partition Size	GP_SIZE_MULT4			12	[154:152]	0h
	GP_SIZE_MULT3				[151:149]	0h
	GP_SIZE_MULT2				[148:146]	0h
	GP_SIZE_MULT1				[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	4GB	J-Option	3	[142:140]	467h
			B-Option			460h
		8GB	J-Option			934h
			B-Option			928h
Enhanced User Data Start Address	ENH_START_ADDR			4	[139:136]	0h
Reserved	-			1	[135]	0h
Bad Block Management mode	SEC_BAD_BLK_MGMNT			1	[134]	0h
Production State Awareness	PRODUCTION_STATE_AWARENESS			1	[133]	0h
Package Case Temperature is controlled	TCASE_SUPPORT			1	[132]	0h
Periodic Wake-Up	PERIODIC_WAKEUP			1	[131]	0h
Program CID/CSD in DDR Mode Support	PROGRAM_CID_CSD_DDR_SUPPORT			1	[130]	1h
Reserved	-			2	[129:128]	0h
Vendor Specific Fields	VENDOR_SPECIFIC_NFIELD			64	[127:64]	–
Native Sector Size	NATIVE_SECTOR_SIZE			1	[63]	0h
Sector Size Emulation	USE_NATIVE_SECTOR			1	[62]	0h
Sector Size	DATA_SECTOR_SIZE			1	[61]	0h
1st Initialization After Disabling Sector Size Emulation	INI_TIMEOUT_EMU			1	[60]	0h
Class 6 Command Control	CLASS_6_CTRL			1	[59]	0h
Number of Addressed Groups To Be Released	DYNCAP_NEEDED			1	[58]	0h
Exception Events Control	EXCEPTION_EVENTS_CTRL			2	[57:56]	0h
Exception Events Status	EXCEPTION_EVENTS_STATUS			2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIBUTE			2	[53:52]	0h

Name	Field			Size (Bytes)	ECSD Bits	ECSD Value(1)
Context Configuration	CONTEXT_CONF			15	[51:37]	-
Packed Command Status	PACKED_COMMAND_STATUS			1	[36]	0h
Packed Command Failure Index	PACKED_FAILURE_INDEX			1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION			1	[34]	0h
Control To Turn The Cache ON/OFF	CACHE_CTRL			1	[33]	0h
Flushing Of The Cache	FLUSH_CACHE			1	[32]	0h
Reserved	-			1	[31]	0h
Mode Config	MODE_CONFIG			1	[30]	0h
Mode Operation Codes	MODE_OPERATION_STATUS			1	[29]	0h
Reserved	-			2	[28:27]	0h
FFU Status	FFU_STATUS			1	[26]	0h
Pre Loading Data Size	PRE_LOADING_DATA_SIZE			4	[25:22]	0h
Max Pre Loading Data Size	MAX_PRE_LOADING_DATA_SIZE	4GB	J-Option	4	[21:18]	7651328
			B-Option			7536640
		8GB	J-Option			15302656
			B-Option			15204352
Product State Awareness Enablement	PRODUCT_STATE_AWARENESS_ENABLEMENT			1	[17]	1h
Secure Removal Type	SECURE_REMOVAL_TYPE			1	[16]	1h
Command Queue Mod Enable	CMQ_MODE_EN			1	[15]	0h
Reserved	-			15	[14:0]	-

Note:

1. Reserved bits should read as “0”.
2. Obsolete values should be don’t care.
3. This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing (see Section 10.6.1 of JESD84-B51). If the host sets value 2 the Device changes its timing to HS200 interface timing (see Section 10.8.1 of JESD84-B51), If the host sets HS_TIMING [3:0] to 0x3, the device changes its timing to HS400 interface timing (see10.10).
4. It is set to ‘0’ (1 bit data bus) after power up and can be changed by a SWITCH command.
5. Could be changed by Firmware.
6. The values of Device version, Cache size, Sector Count, Max Enhanced Area Size, Enhanced User Data Area Size and Max preloading data size are expressed in Decimal, while the value of h is the abbreviation of Hexadecimal.

5.4 RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7. For detailed register setting value, please refer to FAE.

5.5 DSR Register

The 16-bit driver stage register (DSR) is described in detail in Section 7.6 of the JEDEC Standard Specification No.JESD84-B51. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. For detailed register setting value, please refer to FAE.

Table 5.1 eMMC Registers

Name	Width (Bytes)	Description	Implementation
CID	16	Device Identification number, an individual number for identification.	Mandatory
RCA	2	Relative Device Address is the Device system address, dynamically assigned by the host during initialization.	Mandatory
DSR	2	Driver Stage Register, to configure the Device's output drivers.	Optional
CSD	16	Device Specific Data, information about the Device operation conditions.	Mandatory
OCR	4	Operation Conditions Register. Used by a special broadcast command to identify the voltage type of the Device.	Mandatory
EXT_CSD	512	Extended Device Specific Data. Contains information about the Device capabilities and selected modes. Introduced in standard v4.0	Mandatory

6. The eMMC FUNCTIONAL DESCRIPTION

6.1 Pseudo Technology (pSLC)

Each cell in an MLC NAND can be programmed to store 2 bits of data with 4 total voltage states. In Pseudo-SLC (pSLC) mode, the memory cell is used in 1-bit mode, thus resulting in higher endurance, lower error rates and extended temperature range. ISSI firmware optimizes the *eMMC* device with Pseudo technology to achieve industrial and automotive level reliability. For ISSI *eMMC* device, Pseudo SLC (pSLC) mode provides half capacity of MLC mode.

6.2 Field Firmware Update (FFU)

Field Firmware Updates (FFU) enables features enhancement in the field. Using this mechanism, the host downloads a new version of the firmware to the *eMMC* device and, following a successful download, instructs the *eMMC* device to install the new downloaded firmware into the device.

In order to start the FFU process the host first checks if the *eMMC* device supports FFU capabilities by reading SUPPPORTED_MODES and FW_CONFIG fields in the EXT_CSD. If the *eMMC* device supports the FFU feature the host may start the FFU process. The FFU process starts by switching to FFU Mode in MODE_CONFIG field in the EXT_CSD. In FFU Mode host should use closed-ended or open ended commands for downloading the new firmware and reading vendor proprietary data. In this mode, the host should set the argument of these commands to be as defined in FFU_ARG field. In case these commands have a different argument the device behavior is not defined and the FFU process may fail. The host should set Block Length to be DATA_SECTOR_SIZE. Downloaded firmware bundle must be DATA_SECTOR_SIZE size aligned (internal padding of the bundle might be required). Once in FFU Mode the host may send the new firmware bundle to the device using one or more write commands.

The host could regain regular functionality of write and read commands by setting MODE_CONFIG field in the EXT_CSD back to Normal state. Switching out of FFU Mode may abort the firmware download operation. When host switched back to FFU Mode, the host should check the FFU Status to get indication about the number of sectors which were downloaded successfully by reading the NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED in the extended CSD. In case the number of sectors which were downloaded successfully is zero the host should re-start downloading the new firmware bundle from its first sector. In case the number of sectors which were downloaded successfully is positive the host should continue the download from the next sector, which would resume the firmware download operation. In case MODE_OPERATION_CODES field is not supported by the device the host sets to NORMAL state and initiates a CMD0/HW_Reset/Power cycle to install the new firmware. In such case the device doesn’t need to use NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED.

In both cases occurrence of a CMD0/HW_Reset/Power occurred before the host successfully downloaded the new firmware bundle to the device may cause the firmware download process to be aborted.

6.3 Power off Notification for Sleep

The host should notify the device before it powers the device off. This allows the device to better prepare itself for being powered off. Power the device off means to turn off all its power supplies. In particular, the host should issue a power off notification (POWER_OFF_LONG, POWER_OFF_SHORT) if it intends to turn off both VCC and VCCQ power I or it may use to a power off notification (SLEEP_NOTIFICATION) if it intends to turn-off VCC after moving the device to Sleep state.

To indicate to the device that power off notification is supported by the host, a supporting host shall first set the POWER_OFF_NOTIFICATION byte in EXT_CSD [34] to POWERED_ON (0x01). To execute a power off, before powering the device down the host will changes the value to either POWER_OFF_SHORT (0x02) or POWER_OFF_LONG (0x03). Host should wait for the busy line to be de-asserted. Once the setting has changed to either 0x02 or 0x03, host may safely power off the device.

The host may issue SLEEP_AWAKE (CMD5) to enter or to exit from Sleep state if POWER_OFF_NOTIFICATION byte is set to POWERED_ON. Before moving to Standby state and then to Sleep state, the host sets POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and waits for the DAT0 line de-assertion. While in Sleep (slp) state VCC (Memory supply) may be turned off as defined in 4.1.6. Removing power supplies other than VCC while the device is in the Sleep (slp) state may result in undefined device behavior. Before removing all power supplies, the host should transition the device out of Sleep (slp) state back to Transfer state using CMD5 and CMD7 and then execute a power off notification setting POWER_OFF_NOTIFICATION byte to either POWER_OFF_SHORT or POWER_OFF_LONG.

If host continues to send commands to the device after switching to the power off setting (POWER_OFF_LONG, POWER_OFF_SHORT or SLEEP_NOTIFICATION) or performs HPI during its busy condition, the device shall restore the POWER_OFF_NOTIFICATION byte to POWERED_ON.

If host tries to change POWER_OFF_NOTIFICATION to 0x00 after writing another value there, a SWITCH_ERROR is generated.

The difference between the two power-off modes is how urgent the host wants to turn power off. The device should respond to POWER_OFF_SHORT quickly under the generic CMD6 timeout. If more time is acceptable, POWER_OFF_LONG may be used and the device shall respond to it within the POWER_OFF_LONG_TIME timeout.

While POWER_OFF_NOTIFICATION is set to POWERED_ON, the device expects the host to host shall:

- Keep the device power supplies alive (both VCC and VCCQ) and in their active mode
- Not power off the device intentionally before changing POWER_OFF_NOTIFICATION to either POWER_OFF_LONG or POWER_OFF_SHORT
- Not power off VCC intentionally before changing POWER_OFF_NOTIFICATION to SLEEP_NOTIFICATION and before moving the device to Sleep state

Before moving to Sleep state hosts may set the POWER_OFF_NOTIFICATION byte to SLEEP_NOTIFICATION (0x04) if aware that the device is capable of autonomously initiating background operations for possible performance improvements. Host should wait for the busy line to be de-asserted. Busy line may be asserted up the period defined in SLEEP_NOTIFICATION_TIME byte in EXT_CSD [216]. Once the setting has changed to 0x04 host may set the device into Sleep mode (CMD7+CMD5). After getting out from Sleep the POWER_OFF_NOTIFICATION byte will restore its value to POWERED_ON. HPI may interrupt the SLEEP_NOTIFICATION operation. In that case POWER_OFF_NOTIFICATION byte will restore to POWERED_ON.

6.4 Enhanced User Data Area

The *eMMC* supports Enhanced User Data Area feature which allows the User Data Area of *eMMC* to be configured as SLC Mode. Therefore, when host set the Enhanced User Data Area, the area will occupy more size of original set up size. The Max Enhanced User Data Area size is defined as - (MAX_ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The Enhanced use data area size is defined as - (ENH_SIZE_MULT x HC_WP_GRP_SIZE x HC_ERASE_GRP_SIZE x 512 KBytes). The host shall follow the flow chart of JEDEC spec for configuring the parameters of General Purpose Area Partitions and Enhanced User Data Area.

6.5 Write Cache

Cache is a temporary storage space in an *eMMC* device. The cache should in typical case reduce the access time and increase the speed (compared to an access to the main nonvolatile storage). The cache is not directly accessible by the host. This temporary storage space may be utilized also for some implementation specific operations like as an execution memory for the memory controller and/or as storage for an address mapping table etc. However, there is data inconsistence risk when using nonvolatile cache. It’s recommend only turning on the cache for the application which requires not too high reliability.

The cache shall be OFF by default after power up, RST_n assertion or CMD0. All accesses shall be directed to the nonvolatile storage like defined elsewhere in this specification. The cache function can be turned ON and OFF by writing to the CACHE_CTRL byte (EXT_CSD byte [33]). Turning the cache ON shall enable behavior model defined in this section. Turning the cache OFF shall trigger flushing of the data to the nonvolatile storage.

6.6 Cache Enhancement Barrier

Barrier function provides a way to perform a delayed in-order flushing of a cached data. The main motivation for using barrier commands is to avoid the long delay that is introduced by flush commands. There are cases where the host is not interested in flushing the data right away, however it would like to keep an order between different cached data batches. The barrier command enables the host achieving the in-order goal but without paying the flush delay, since the real flushing can be delayed by the device to some later idle time. The formal definition of the barrier rule is as follows:

Denote a sequence of requests Ri, i=0,..,N. Assuming a barrier is set between requests Rx and Rx+1 (0<x<N) then all the requests R0..Rx must be flushed to the non-volatile memory before any of the requests Rx+1..RN. Between two barriers the device is free to write data into the non-volatile memory in any order. If the host wants to preserve a certain order it shall flush the cache or set another barrier at a point where order is important.

The barrier is set by writing to the BARRIER bit of the FLUSH_CACHE byte (EXT_CSD byte [32]). Any error resulted can be read from the status register by CMD13 after the completion of the programming as defined for a normal write request. The error could affect any data written to the cache since the previous flush operation.

The device shall support any number of barrier commands between two flush commands. In case of multiple barrier commands between two flush commands a subset of the cached data may be committed to the non-volatile memory according to the barrier rule. Internally, a device may have an upper limit on the barrier amount it can absorb without flushing the cache. That is, if the host exceeds this barrier amount, the device may issue, internally, a normal flush.

The device shall expose its barrier support capability via the BARRIER_SUPPORT byte (EXT_CSD byte [486]). If a device does not support barrier function this register shall be zero. If a device supports barrier function this register shall be one.

Assuming the device supports barrier function, if the BARRIER bit of the FLUSH_CACHE byte is set, a barrier operation shall be executed.

If the cache gets totally full and/or the cache is not able to receive the data of the next access (per block count indicated in CMD23 or per initiated single / open ended multiple block write in general) then it shall still be the responsibility of the *eMMC* device to store the data of the next access within the timeouts that are specified elsewhere in this specification. The actual algorithm to handle the new data and possible flush of some older cached data is left for the implementation.

Note: When issuing a force-programming write request (CMD23 with bit 24 on) or a reliable write request (CMD23 with bit 31 on), the host should be aware that the data will be written to the non-volatile memory, potentially, before any cached data, even if a barrier command was issued. Therefore, if the writing order to the non-volatile memory is important, it is the responsibility of the host to issue a flush command before the force-programming or the reliable-write request.

In order to use the barrier function, the host shall set bit 0 of BARRIER_EN (EXT_CSD byte [31]). The barrier feature is optional for an *eMMC* device.

6.7 Cache Flushing Policy

The host may require the device to flush data from the cache in an in-order manner. From time to time, to guarantee in-order flushing, the host may command the device to flush the device cache or may use a barrier command.

However, if the *eMMC* device flushing policy is to flush data from the cache in an in-order manner, cache barrier commands or flush commands operations (In case goal is to guarantee the flushing order) are redundant and impose a needless overhead to the device and host.

FIFO bit in CACHE_FLUSH_POLICY field (EXT_CSD byte [240]) is used by the device to indicate to the host that the device cache flushing policy is First-In-First-Out; this means that the device guarantees that the order of the flushing of data would be the in same order which data was written to the cache. When the FIFO bit is set it is recommended for the host not to send cache barrier commands or flush operations which goal is to guarantee the flushing order as they are redundant and impose a burden to the system.

However, if the FIFO bit is set to 1b and the device supports the cache barrier mechanism, the host may still send barrier commands without getting an error. Sending these commands will not change the device behavior as device flushes cache in-order anyway.

The CACHE_FLUSH_POLICY field is read-only field and never change its value either by the host or device.

6.8 Production State Awareness (PSA)

eMMC device could utilize the information of whether it is in production environment and operate differently than it operates in the field.

For example, content that was loaded into the storage device prior to soldering might get corrupted, at higher probability, during device soldering. The *eMMC* device could use “special” internal operations for loading content prior to device soldering that would reduce production failures and use “regular” operations post-soldering.

PRODUCTION_STATE_AWARENESS [133] field in extended CSD is used as a mechanism through which the host should report to the device whether it is pre or post soldering state.

This standard defines two methods, Manual Mode and Auto Mode, to manage the device production state.

The trigger for starting or re-starting the process is setting correctly PRE_LOADING_DATA_SIZE field. Before setting this field the host is expected to make sure that the device is clean and any data that was written before to the device is expected to be erased using CMD35, CMD36 and CMD38.

In case the host erased data, overrode existing data or performed re-partition during production state awareness it should restart the production state awareness process by re-setting PRE_LOADING_DATA_SIZE.

6.9 Boot Operation

Device supports not only boot mode but also alternative boot mode. Device supports high speed timing and dual data rate during boot.

.

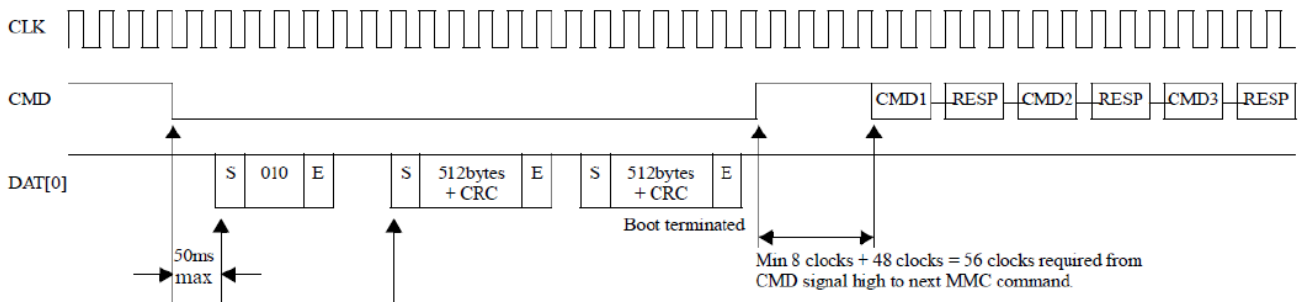
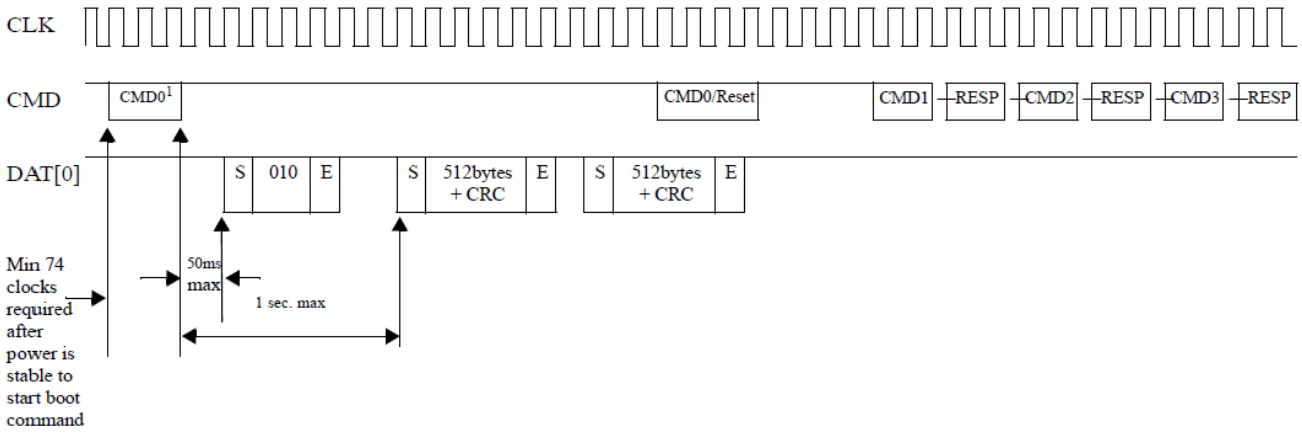


Figure 6.1 eMMC State Diagram (boot mode)



Note:

1. Applied CMD0 with argument 0xFFFFFFFA

Figure 6.2 eMMC State Diagram (alternative boot mode)

Table 6.1 Boot Ack, Boot Data and Initialization Time

Timing Factor	Value
Boot ACK Time	< 50 ms
Boot Data Time	< 100 ms
Initialization Time (1)	< 3 secs

Note:

1. This initialization time includes partion setting. Please refer to INI_TIMEOUT_AP in Extended CSD Register. Normal initialization time (without partition setting) is controlled within 1 sec.

7. POWER-UP

7.1 eMMC POWER-UP

An *eMMC* bus power-up is handled locally in each device and in the bus master. 7.1 shows the power-up sequence and is followed by specific instructions regarding the power-up sequence. Refer to section 10.1 of the JEDEC Standard Specification No.JESD84-B51 for specific instructions regarding the power-up sequence.

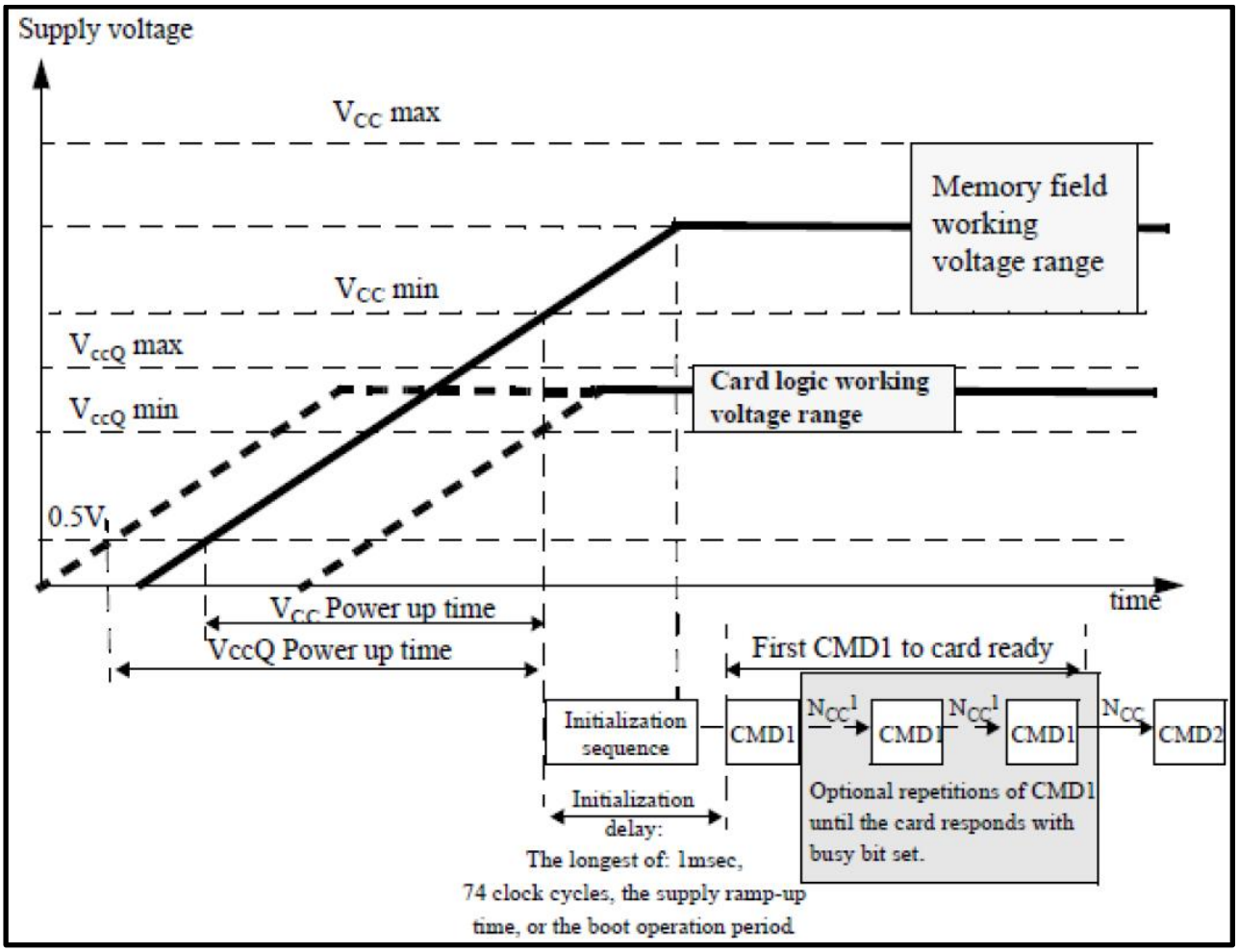


Figure 7.1 eMMC POWER-UP Diagram

7.2 eMMC POWER-CYCLING

The master can execute any sequence of V_{CC} and V_{CCQ} power-up/power-down. However, the master must not issue any commands until V_{CC} and V_{CCQ} are stable within each operating voltage range. After the slave enters sleep mode, the master can power-down V_{CC} to reduce power consumption. It is necessary for the slave to be ramped up to V_{CC} before the host issues CMD5 (SLEEP_AWAKE) to wake the slave unit. For more information about power cycling see Section 10.1.3 of the JEDEC Standard Specification No.JESD84-B51.

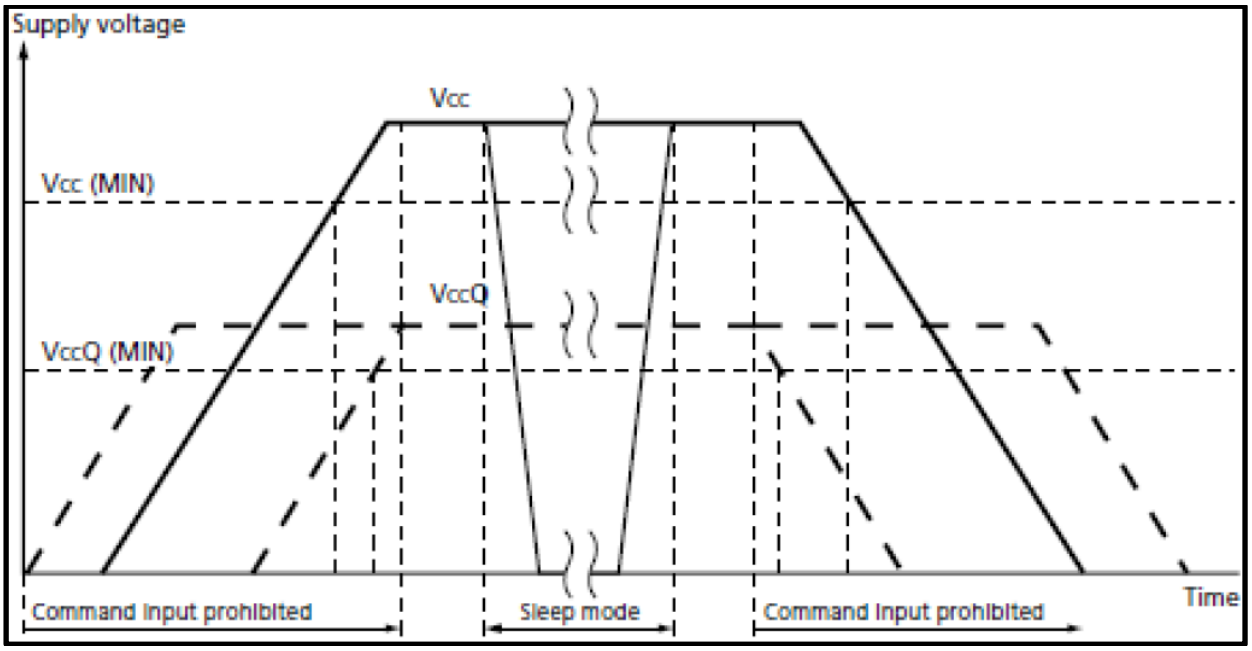


Figure 7.2 eMMC POWER-CYCLE

8. ELECTRICAL CHARACTERISTICS

8.1 ABSOLUTE MAXIMUM RATINGS (1) POWER CONSUMPTION

Input Voltage	-0.6V to +4.6V
V_{CC} Supply	-0.6V to +4.6V
V_{CCQ} Supply	-0.6V to +4.6V

Note:

2. Applied conditions greater than those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8.2 Operating Conditions

Parameter		Symbol	Min	Max.	Unit	Remark
Ambient Temperature	I Grade		-40	85	℃	
	A2 Grade		-40	105		
Max. Case Temperature	I Grade		-	95		
	A2 Grade		-	115		
Non-Operating Temperature	I Grade		-40	85		3
	A2 Grade		-40	105		3
Peak voltage on all lines						
All Inputs						
Input Leakage Current (before initialization sequence and/or the internal pull up resistors connected)			-100	100	µA	
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)			-2	2	µA	
All Outputs						
Output Leakage Current (before initialization sequence)			-100	100	µA	
Output Leakage Current (after initialization sequence)			-2	2	µA	

Notes:

1. Initialization sequence is defined in Section 10.1 of the JEDEC Standard Specification No.JESD84-B51.
2. DS (Data Strobe) pin is excluded.
3. After being soldered onto PCBA.

8.2.1 POWER SUPPLY: *eMMC*

In the eMMC, VCC is used for the NAND flash device and its interface voltage; VCCQ is for the controller and the MMC interface voltage as shown in Figure 8.1. The core regulator is optional and only required when internal core logic voltage is regulated from VCCQ. A CReg capacitor must be connected to the VDDi terminal to stabilize regulator output on the system.

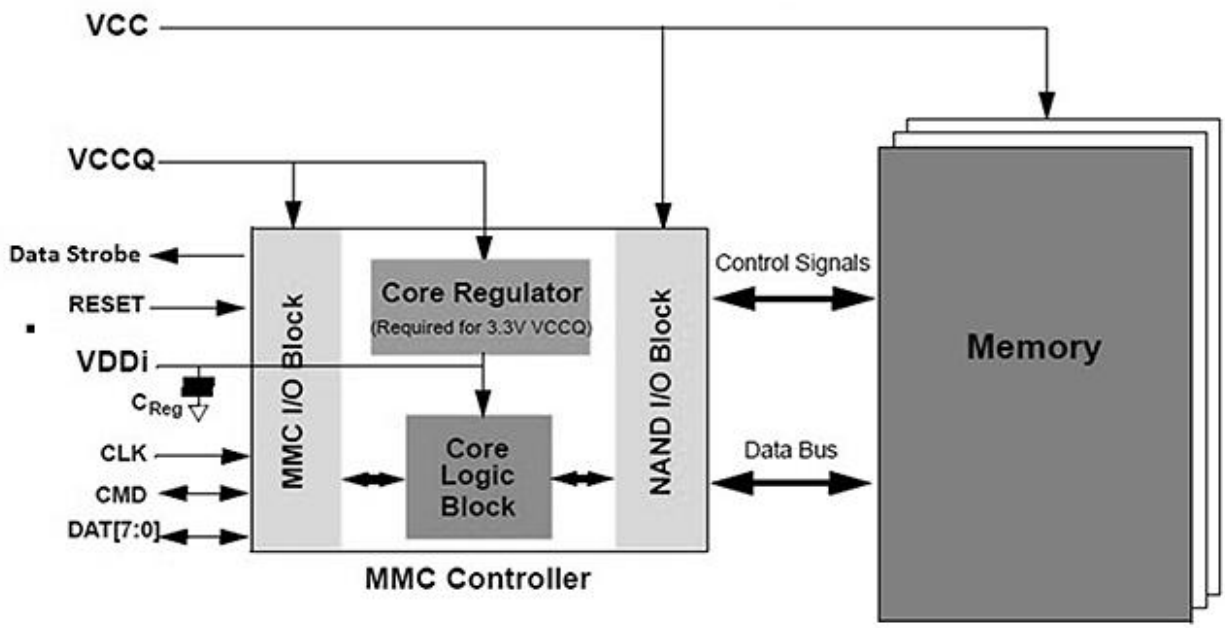


Figure 8.1 eMMC Internal Power Diagram

8.2.2 eMMC Power Supply Voltage

The *eMMC* supports one or more combinations of V_{CC} and V_{CCQ} as shown in **Table** 8.1. The VCCQ must be defined at equal to or less than VCC.

Table 8.1 *eMMC* Operating Voltage

Parameter	Symbol	MIN	MAX	Unit	Remarks
Supply voltage (NAND)	V_{CC}	2.7	3.6	V	
Supply voltage (I/O)	V_{CCQ}	2.7	3.6	V	
		1.7	1.95	V	
Supply power-up for 3.3V	t_{PRUH}		35	ms	
Supply power-up for 1.8V	t_{PRUL}		25	ms	

The *eMMC* must support at least one of the valid voltage configurations, and can optionally support all valid voltage configurations.

Table 8.2 *eMMC* Voltage Combinations

		V_{CCQ}	
		1.7V–1.95V	2.7V–3.6V[1]
Vcc	**2.7V-3.6V**	Valid	Valid

Note:

1. V_{CCQ} (I/O) 3.3 volt range is not supported in HS200 /HS400 devices.

8.2.3 BUS SIGNAL LINE LOAD

The total capacitance C_L of each line of the *eMMC* bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of *eMMC* connected to this line:
$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$
The sum of the host and bus capacitances must be under 20pF.

Table 8.3 Signal Line Load

Parameter	Symbol	Min	Max	Unit	Remark
Pull-up resistance for CMD	R_{CMD}	4.7	50	Kohm	to prevent bus floating
Pull-up resistance for DAT0–7	R_{DAT}	10	50	Kohm	to prevent bus floating
Bus signal line capacitance	CL		30	pF	Single Device
Single Device capacitance	C_{DEVICE}		6	pF	
Maximum signal line inductance			16	nH	
V_{CCQ} decoupling capacitor		2.2+0.1	4.7+0.22	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
VCC capacitor value		1+0.1	4.7+0.22	µF	It should be located as close as possible to the balls defined in order to minimize connection parasitic
V_{DDi} capacitor value	C_{REG}	1	4.7+0.1	µF	To stabilize regulator output to controller core logics. It should be located as close as possible to the balls defined in order to minimize connection parasitic

8.2.4 HS400 REFERENCE LOAD

The circuit in Figure 8.2 shows the reference load used to define the HS400 Device Output Timings and overshoot / undershoot parameters.
The reference load is made up by the transmission line and the $C_{REFERENCE}$ capacitance.
The reference load is not intended to be a precise representation of the typical system environment nor a depiction of the actual load presented by a production tester.
System designers should use IBIS or other simulation tools to correlate the reference load to system environment. Manufacturers should correlate to their production test conditions.
Delay time (td) of the transmission line has been introduced to make the reference load independent from the PCB technology and trace length.

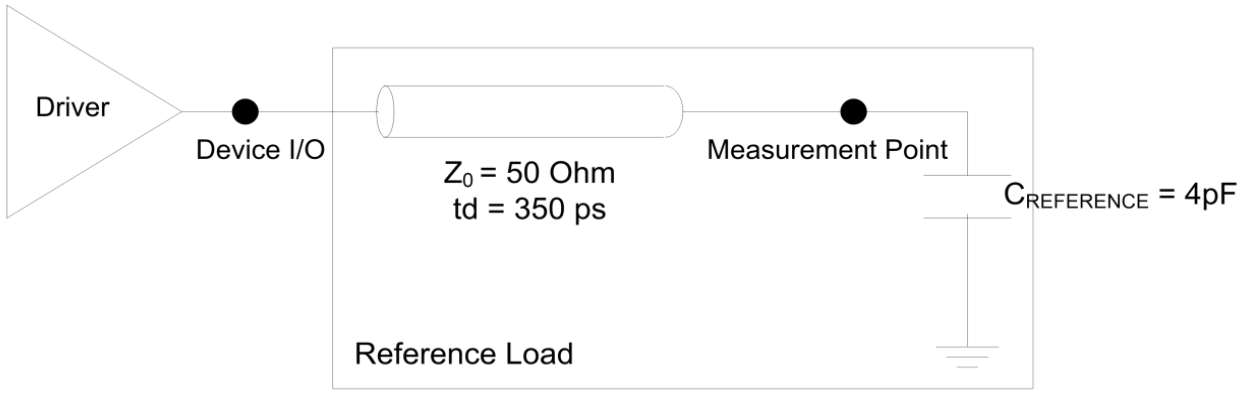


Figure 8.2 HS400 Reference Load

8.3 BUS SIGNAL LEVELS

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

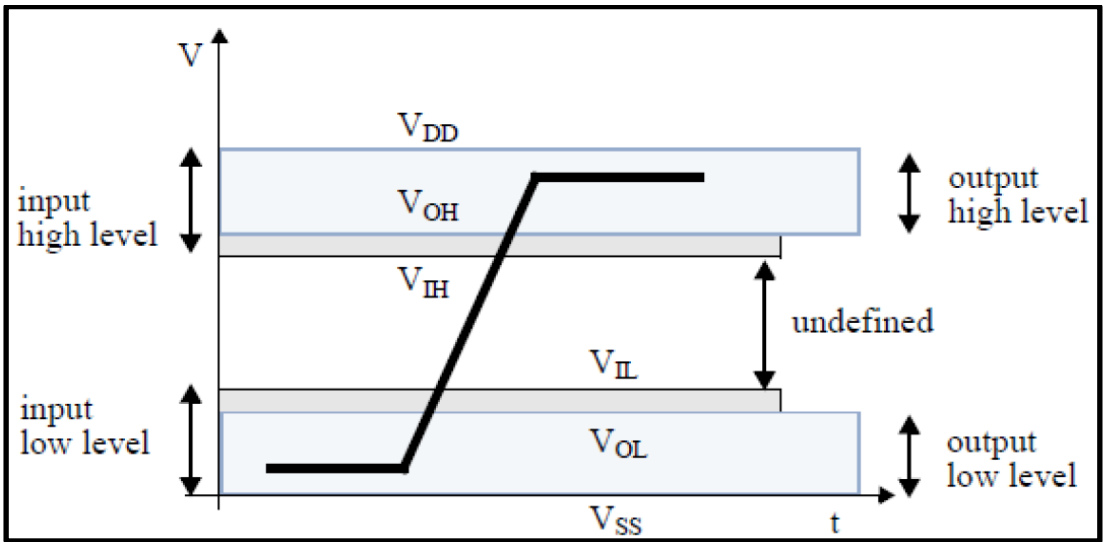


Figure 8.3 BUS Signal Levels

8.3.1 BUS SIGNAL LINE LOAD

The total capacitance C_L of each line of the *eMMC* bus is the sum of the bus master capacitance C_{HOST}, the bus capacitance C_{BUS} itself and the capacitance C_{DEVICE} of *eMMC* connected to this line:
$C_L = C_{HOST} + C_{BUS} + C_{DEVICE}$
The sum of the host and bus capacitances must be under 20pF.

Table 8.4 Open-drain Bus Signal Level

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V_{CCQ} – 0.2		V	IOH = -100 µA
Output LOW voltage	VOL		0.3	V	IOL = 2 mA

The input levels are identical with the push-pull mode bus signal levels.

8.3.2 PUSH-PULL MODE BUS SIGNAL LEVEL-eMMC

The device input and output voltages shall be within the following specified ranges for any V_{DD} of the allowed voltage range
For 2.7V-3.6V V_{CCQ} range (compatible with JESD8C.01)

Table 8.5 Push-pull Signal Level—High-voltage *eMMC*

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	0.75 * V_{CCQ}		V	IOH = -100 µA @ V_{CCQ} min
Output LOW voltage	VOL		0.125 * V_{CCQ}	V	IOL = 100 µA @ V_{CCQ} min
Input HIGH voltage	VIH	0.625 * V_{CCQ}	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	VSS – 0.3	0.25 * V_{CCQ}	V	

For 1.70V – 1.95V V_{CCQ} range (: Compatible with EIA/JEDEC Standard "EIA/JESD8-7 Normal Range" as defined in the following table.

Table 8.6 Push-pull Signal Level—1.70 -1.95 V_{CCQ} Voltage Range

Parameter	Symbol	Min	Max.	Unit	Conditions
Output HIGH voltage	VOH	V_{CCQ} – 0.45V		V	IOH = -2mA
Output LOW voltage	VOL		0.45V	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V_{CCQ} [1]	V_{CCQ} + 0.3	V	
Input LOW voltage	VIL	V_{SS} – 0.3	0.35 * V_{CCQ} [2]	V	

Notes:

1. 0.7 * V_{DD} for MMC™4.3 and older revisions /HS400 devices.
2. 0.3 * V_{DD} for MMC™4.3 and older revisions.

8.3.3 BUS OPERATING CONDITIONS for HS200 & HS400

The bus operating conditions for HS200 devices is the same as specified in sections 10.5.1 of JESD84-B51 through 13.5.2 of JESD84-B51. The only exception is that V_{CCQ}=3.3v is not supported.

8.3.4 BUS DEVICE OUTPUT DRIVER REQUIREMENTS for HS200 & 400

Refer to section 10.5.4 of the JEDEC Standard Specification No.JESD84-B51.

8.4 BUS TIMING

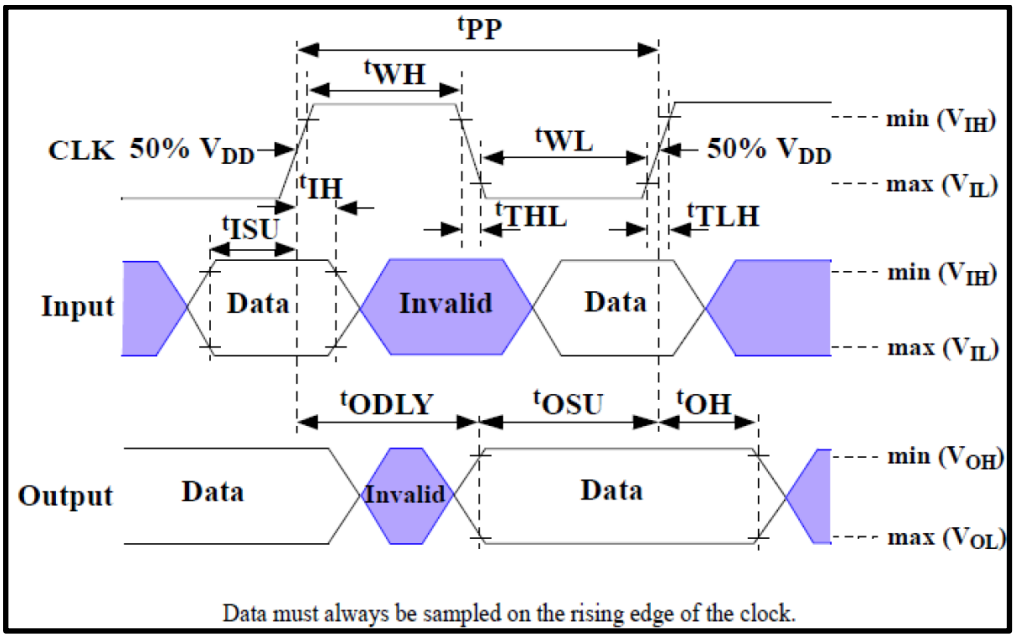


Figure 8.4 BUS Timing Diagram

8.5 DEVICE INTERFACE TIMIMG

Table 8.7 High-speed Device Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	fPP	0	52[3]	MHz	CL ≤ 30 pF Tolerance:+100KHz
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	Tolerance: +20KHz
Clock high time	tWH	6.5		ns	CL ≤ 30 pF
Clock low time	tWL	6.5		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		3	ns	CL ≤ 30 pF
Clock fall time	tTHL		3	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output delay time during data transfer	tODLY		13.7	ns	CL ≤ 30 pF
Output hold time	tOH	2.5		ns	CL ≤ 30 pF
Signal rise time[5]	tRISE		3	ns	CL ≤ 30 pF
Signal fall time	tFALL		3	ns	CL ≤ 30 pF

Notes:

1. CLK timing is measured at 50% of VDD devices.
2. eMMC shall support the full frequency range from 0-26Mhz or 0-52MH.
3. Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. Inputs CMD DAT rise and fall times are measured by min (VIH) and max (VIL) and outputs CMD DAT rise and fall times are measured by min (VOH) and max (VOL).

Table 8.8 Backward-compatible Device Interface Timing

Clock CLK [2]					
Clock frequency Data Transfer Mode (PP)[3]	fPP	0	26	MHz	CL ≤ 30 pF
Clock frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10			CL ≤ 30 pF
Clock low time	tWL	10		ns	CL ≤ 30 pF
Clock rise time[4]	tTLH		10	ns	CL ≤ 30 pF
Clock fall time	tTHL		10	ns	CL ≤ 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	tISU	3		ns	CL ≤ 30 pF
Input hold time	tIH	3		ns	CL ≤ 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time[5]	tOSU	11.7		ns	CL ≤ 30 pF
Output hold time[5]	tOH	8.3		ns	CL ≤ 30 pF

Notes:

1. The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.
2. CLK timing is measured at 50% of VDD.
3. For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.
4. CLK rise and fall times are measured by min (VIH) and max (VIL).
5. tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its application notes.

8.6 BUS TIMING FOR DAT SIGNALS DURING DUAL DATA RATE OPERATION

These timings apply to the DAT [7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operate synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in section 10.5 of JEDEC Standard Specification No.JESD84-B51, therefore there is no timing change for the CMD signal.

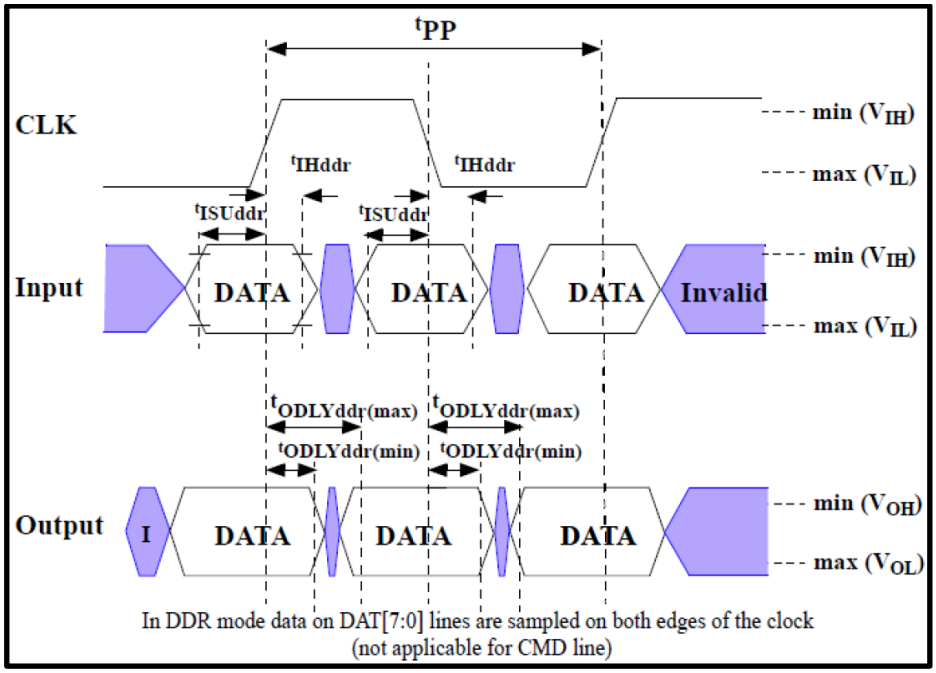


Figure 8.5 Timing Diagram; Data Input/Output in Dual Data Rate Mode

8.6.1 DUAL DATA RATE INTERFACE TIMINGS

Table 8.9 – High-speed Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Input CLK[1]					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	tISUddr	2.5		ns	CL ≤ 20 pF
Input hold time	tIHddr	2.5		ns	CL ≤ 20 pF
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	tODLYddr	1.5	7	ns	CL ≤ 20 pF
Signal rise time (all signals)[2]	tRISE		2	ns	CL ≤ 20 pF
Signal fall time (all signals)	tFALL		2	ns	CL ≤ 20 pF

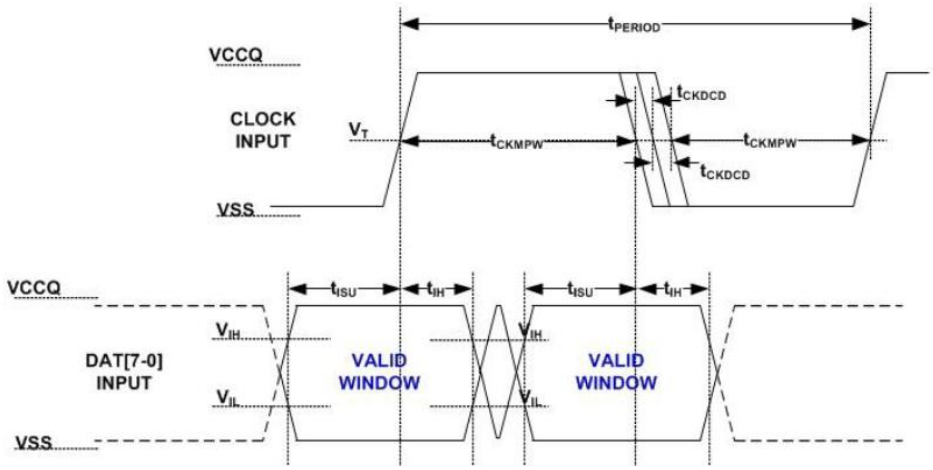
Notes:

1. CLK timing is measured at 50% of VDD.
2. Inputs CMD, DAT rise and fall times are measured by min (V_{IH}) and max (V_{IL}), and outputs CMD, DAT rise and fall times are measured by min (V_{OH}) and max (V_{OL})

8.7 BUS TIMING SPECIFICATION IN HS400 MODE

DUAL DATA RATE INTERFACE TIMINGS

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode. Figure 8.6 and Table 8.10 show Device input timing.



Notes:

1. t_{ISU} and t_{IH} measured at V_{IL}(max.) and V_{IH}(min.).
2. V_{IH} denotes V_{IH}(min.) and V_{IL} denotes V_{IL}(max.).

Figure 8.6 HS400 Device Data Input Timing

Table 8.10 HS400 Device input timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	tPERIOD	5			200MHz (Max), between rising edges With respect to VT.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.
Duty cycle distortion	tCKDCD	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to VT. Includes jitter, phase
Minimum pulse width	tCKMPW	2.2		ns	With respect to VT.
Input DAT (referenced to CLK)					
Input set-up time	tISUddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Input hold time	tIHddr	0.4		ns	CDevice ≤ 6pF With respect to VIH/VIL.
Slew rate	SR	1.125		V/ns	With respect to VIH/VIL.

8.7.1 HS400 DEVICE OUTPUT TIMING

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response

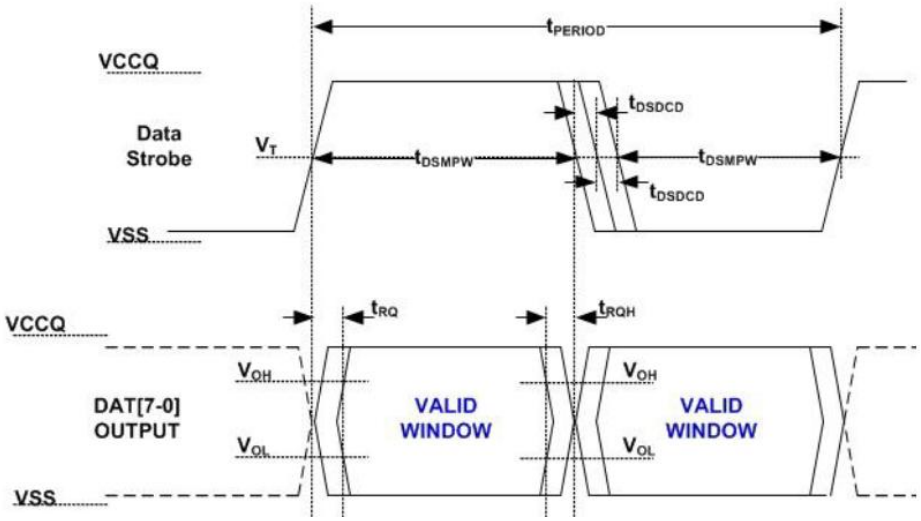


Figure 8.7 HS400 Device Output Timing

Table 8.11 HS400 Device Output timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	tPERIOD	5			200MHz(Max), between rising edges With respect to VT
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load
Duty cycle distortion	tDSDCD	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion (tCKDCD) With respect to VT Includes jitter, phase noise
Minimum pulse width	tDSMPW	2.0		ns	With respect to VT
Read pre-amble	tRPRE	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Read post-amble	tRPST	0.4	-	tPERIOD	Max value is specified by manufacturer. Value up to infinite is valid
Output DAT (referenced to Data Strobe)					
Output skew	tRQ		0.4	ns	With respect to VOH/VOL and HS400 reference load
Output hold skew	tRQH		0.4	ns	With respect to VOH/VOL and HS400 reference load.
Slew rate	SR	1.125		V/ns	With respect to VOH/VOL and HS400 reference load

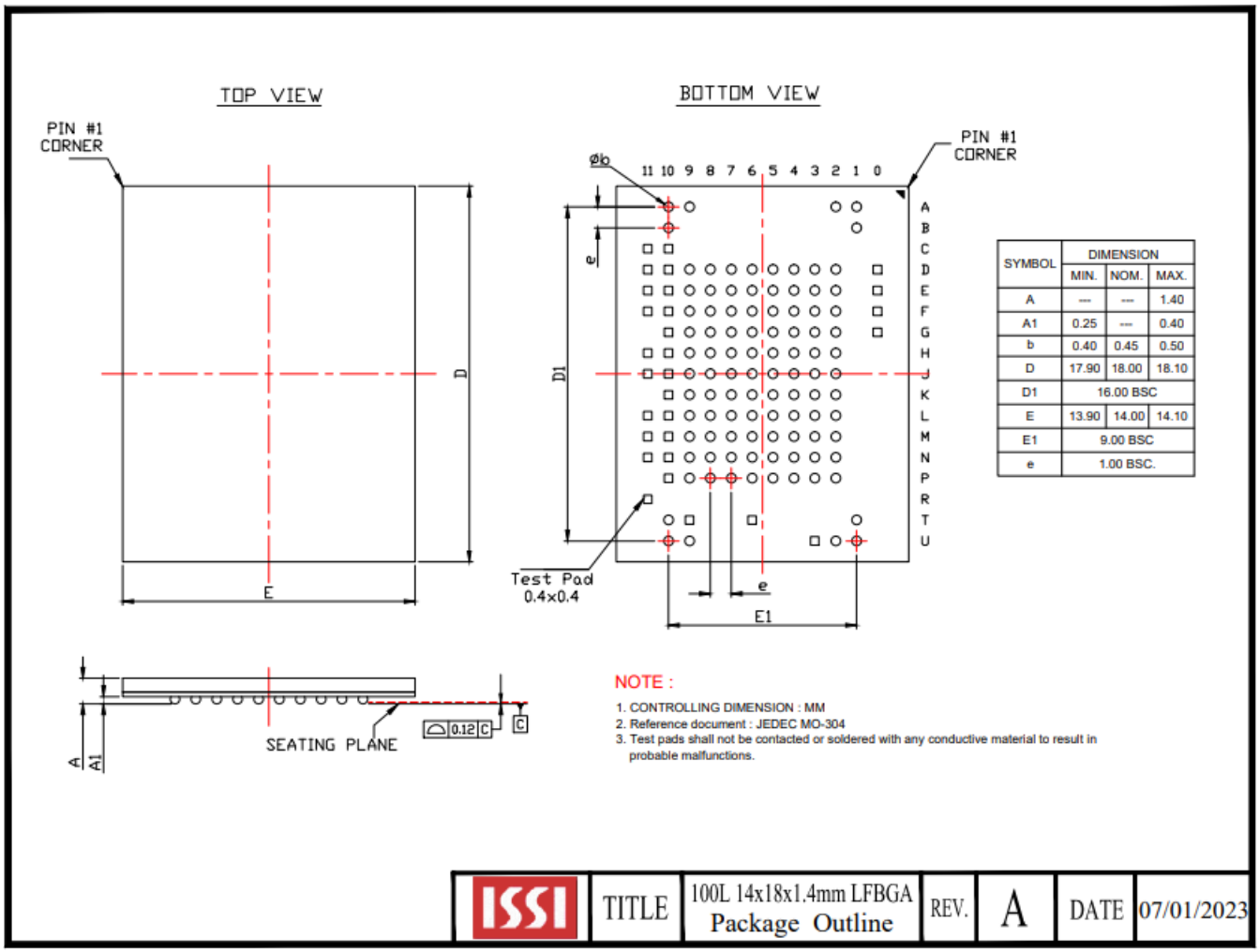
NOTE 1: Measured with HS400 reference load

Table 8.12 – HS400 Capacitance

Parameter	Symbol	Min	Type	Max	Unit	Remark
Pull-up resistance for CMD	RCMD	4.7		100(1)	Kohm	
Pull-up resistance for DAT0-7	RDAT	10		100(1)	Kohm	
Pull-down resistance for Data Strobe	RDS	10		100(1)	Kohm	
Internal pull up resistance DAT1-DAT7	Rint	10		150	Kohm	
Single Device capacitance	CDevice			6	pF	

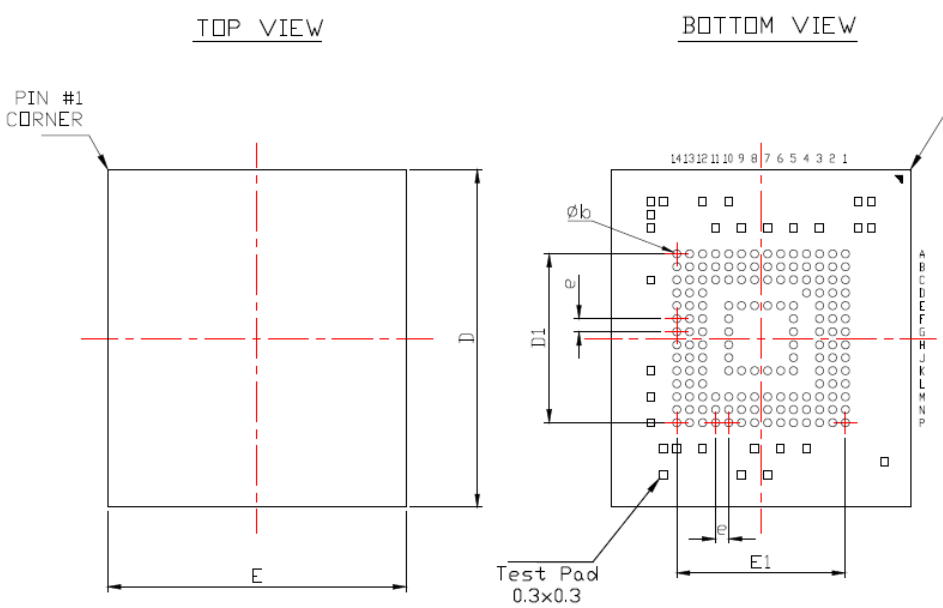
9. PACKAGE TYPE INFORMATION

9.1 100-ball FBGA Package (Q)

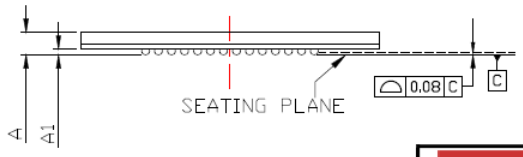


SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	---	---	1.40
A1	0.25	---	0.40
b	0.40	0.45	0.50
D	17.90	18.00	18.10
D1	16.00 BSC		
E	13.90	14.00	14.10
E1	9.00 BSC		
e	1.00 BSC.		

9.2 153-BALL FBGA Package (C)



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	—	—	1.00
A1	0.15	—	—
b	0.25	0.30	0.35
D	12.90	13.00	13.10
D1	6.50 BSC		
E	11.40	11.50	11.60
E1	6.50 BSC		
e	0.50 BSC		



NOTE :

1. CONTROLLING DIMENSION : MM
2. Reference document : JEDEC MO-276
3. Test pads shall not be contacted or soldered with any conductive material to result in probable malfunctions.

ISSI	TITLE	153L 11.5x13x1.0mm VFBGA Package Outline	REV.	B	DATE	03/12/2024

10. ORDERING INFORMATION – Valid Part Numbers

IS 21 E F 08G P _ - J C L I

TEMPERATURE RANGE
I = Industrial (-40°C to +85°C)
A2 = Automotive Grade (-40°C to +105°C)

PACKAGING CONTENT
L = Green Package (RoHS Compliant, Halogen-free) and TSCA Compliant

PACKAGE Type
C = 153-ball FBGA
Q = 100-ball FBGA

OPTION
J = Standard (Boot Partition Size: 4MB)
B = Boot Partition Size: 16MB

Generation.
Blank = 1st Gen.

Pre-Configuration.
P = Pre-Configured in pSLC mode.
Blank = No Pre-Configuration.

eMMC Density
04G = 4 GB
08G = 8 GB

INTERFACE
F = eMMC 5.1

Technology
E = ISSI eMMC with MLC NAND

Product Family
21 = Managed NAND
22 = Automotive Managed NAND

BASE PART NUMBER
IS = Integrated Silicon Solution Inc.

Density	Interface	NAND Flash	Package	Temp. Grade	Order Part Number
4GB	eMMC 5.1	64Gbx1	100 FBGA	I-Temp.	IS21EF04GP-JQLI
					IS21EF04GP-BQLI
				Automotive, A2[1]	IS22EF04GP-JQLA2
					IS22EF04GP-BQLA2
			153 FBGA	I-Temp.	IS21EF04GP-JCLI
					IS21EF04GP-BCLI
				Automotive, A2[1]	IS22EF04GP-JCLA2
					IS22EF04GP-BCLA2
8GB	eMMC 5.1	64Gbx2	100 FBGA	I-Temp.	IS21EF08GP-JQLI
					IS21EF08GP-BQLI
				Automotive, A2[1]	IS22EF08GP-JQLA2
					IS22EF08GP-BQLA2
			153 FBGA	I-Temp.	IS21EF08GP-JCLI
					IS21EF08GP-BCLI
				Automotive, A2[1]	IS22EF08GP-JCLA2
					IS22EF08GP-BCLA2

Note:
1. A2: Meets AEC-Q100 requirements with PPAP.