SST38VF640XB

SST38VF640XB Family
Silicon Errata and Data Sheet Clarifications

The SST38VF640XB family devices that you have received conform functionally to the current device data sheet (DS20005002**E**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (A).

Data sheet clarifications and corrections start on Page 3, following the discussion of silicon issues.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID (in Hex)	Silicon Revision
SST38VF6401B	0xBF, 0x227E, 0x220C, 0x2200	A
SST38VF6402B	0xBF, 0x227E, 0x220C, 0x2201	A
SST38VF6403B	0xBF, 0x227E, 0x2210, 0x2200	A
SST38VF6404B	0xBF, 0x227E, 0x2210, 0x2201	A

TABLE 2: SILICON ISSUE SUMMARY

Item Number	Module	Issue Summary	Affected Revisions(1)
1.	Software ID Entry	Software ID Entry command will be ignored under specific operating conditions.	A
2.	CFI Entry	CFI Entry command will be ignored under specific operating conditions.	A
3.	Security ID Entry	Security ID Entry command will be ignored under specific operating conditions.	A
4.	Volatile Block Protection Entry	Volatile Block Protection Entry command will be ignored under specific operating conditions.	A
5.	WE Controlled Program/Erase Cycle	Unexpected pulse on DQ0 occurs in response to the /OE pin being brought low after initiating a WE Controlled Program/Erase cycle.	A

Note 1: Only the issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous and current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision (**A**).

1. Module: Software ID Entry

When a word program command to program data of 0xXX98 at address locations 0xXXXX55 is followed at any later time by a Software ID Entry command for product identification, the Software ID Entry command fails.

Work around

Prior to issuing a Software ID Entry command, a hardware reset using /RST pin must be performed. A software reset (Addr = XXH, Data = F0H) instead of a hardware reset does not work in this condition.

Affected Silicon Revisions

A						
X						

2. Module: CFI Entry

When a word program command to program data of 0xXX98 at address locations 0xXXXX55 is followed at any later time by a CFI Entry command for reading CFI data, the CFI ID Entry command fails.

Work around

Prior to issuing a CFI Entry command, a hardware reset using the /RST pin must be performed. A software reset (Addr = XXH, Data = F0H) instead of a hardware reset does not work in this condition.

Affected Silicon Revisions

A						
X						

3. Module: Security ID Entry

When a word program command to program data of 0xXX98 at address locations 0xXXXX55 is followed at any later time by a Security ID Entry command for reading Security data, the Security ID Entry command fails.

Work around

Prior to issuing a Security ID Entry command, a hardware reset using /RST pin must be performed. A software reset (Addr = XXH, Data = F0H) instead of a hardware reset does not work in this condition.

Affected Silicon Revisions

A						
X						

4. Module: Volatile Block Protection Entry

When a word program command to program data of 0xXX98 at address locations 0xXXXX55 is followed at any later time by a Volatile Block Protection Entry command for volatile block protection commands, the Volatile Block Protection Entry command fails.

Work around

Prior to issuing a Volatile Block Protection Entry command, a hardware reset using /RST pin must be performed. A software reset (Addr = XXH, Data = F0H) instead of a hardware reset does not work in this condition.

Affected Silicon Revisions

A						
X						

5. Module: WE Controlled Program/Erase Cycle

When a program or erase command using the WE Controlled program cycle is initiated, and the /OE pin is brought low while the device is busy with internal program/erase as indicated by /RDBY pin (Ready/Busy pin), an unexpected pulse on DQ0 is observed.

Work around

Do not bring the /OE pin low until the WE Controlled program/erase cycle has completed and the /RDBY pin is high.

Affected Silicon Revisions

A						
X						

Data Sheet Clarifications

A						
X						

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS20005002**E**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Revision E (09/2025)

Added /WE controlled Program/Erase cycle and /OE Output enable pin requirement.

Revision D (12/2017)

Minor editorial updates to module Work Around sections.

Revision C (11/2017)

Minor editorial updates to Silicon Errata Issues section.

Revision B (10/2017)

Silicon revision update.

Revision A (10/2017)

Initial release of this document; Issued for silicon issues 1-4.

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ISBN: 979-8-3371-1934-2

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