EEPROM Serial 1-Mb I^{2}C

CAT24M01LV

Description

The CAT24M01LV is a EEPROM Serial 1-Mb I^{2}C, internally organized as 131,072 words of 8 bits each.

It features a 256-byte page write buffer and supports the Standard (100 kHz), Fast (400 kHz) and Fast-Plus (1 MHz) I^{2}C protocol.

Write operations can be inhibited by taking the WP pin High (this protects the entire memory).

External address pins make it possible to address up to four CAT24M01LV devices on the same bus.

On-Chip ECC (Error Correction Code) makes the device suitable for high reliability applications.

Features

- Supports Standard, Fast and Fast-Plus I^{2}C Protocol
- 1.7 V to 5.5 V Supply Voltage Range
- 256-Byte Page Write Buffer
- Hardware Write Protection for Entire Memory
- Schmitt Triggers and Noise Suppression Filters on I^{2}C Bus Inputs (SCL and SDA)
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial and Extended Temperature Range
- 8-pin, SOIC, TSSOP and 8-pad UDFN Packages
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

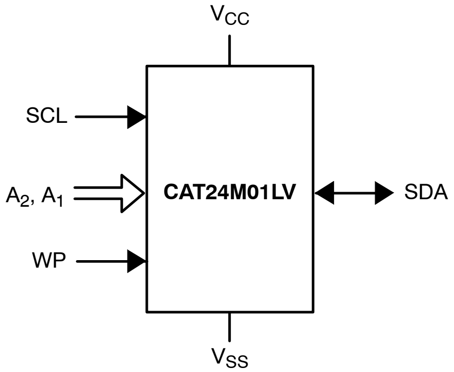
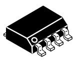


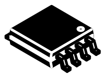
Figure 1. Functional Symbol

This document contains information on some products that are still under development. **onsemi** reserves the right to change or discontinue these products without notice.

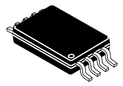


SOIC-8
DW SUFFIX
CASE 751BD

UDFN-8
MU3 SUFFIX
CASE 517BU

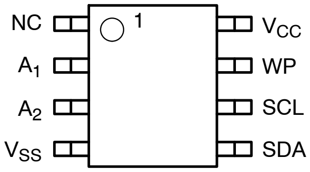


SOIC-8 WIDE
DX SUFFIX
CASE 751BE



TSSOP-8
DT SUFFIX
CASE 948AL

PIN CONFIGURATION



SOIC (W, X), TSSOP (Y),
UDFN (HU5)

For the location of Pin 1, please consult the corresponding package drawing.

PIN FUNCTION

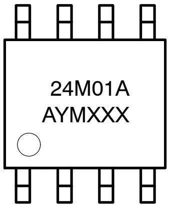
Pin Name	Function
A_1, A_2	Device Address
SDA	Serial Data
SCL	Serial Clock
WP	Write Protect
V_{CC}	Power Supply
V_{SS}	Ground

ORDERING INFORMATION

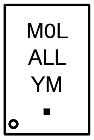
See detailed ordering and shipping information on page 9 of this data sheet.

August, 2025 − Rev. 2

MARKING DIAGRAMS



(SOIC-8)



(UDFN-8)

24M01A = Specific Device Code
A = Assembly Location
Y = Production Year (Last Digit)
M = Production Month (1−9, O, N, D)
XXX = Last Three Digits of Assembly Lot Number

M0L = Specific Device Code
A = Assembly Location Code
LL = Assembly Lot Number
Y = Year
M = Month
▪ = Pb-Free Package

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Unit
Storage Temperature	–65 to +150	°C
Voltage on any Pin with Respect to Ground (Note 1)	–0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Unit
N_{END} (Notes 3, 4)	Endurances	1,000,000	Program/Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
3. Test Condition: Page Mode, V_{CC} = 5 V, 25 °C.
4. The device uses ECC (Error Correction Code) logic with 6 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re-programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

Table 3. D.C. OPERATING CHARACTERISTICS

V_{CC} = 1.7 V to 5.5 V, T_A = −40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Max	Unit
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz / 1 MHz			1	mA
I_{CCW}	Write Current				8.0	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40 °C to +85 °C		2	µA
			T_A = −40 °C to +125 °C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40 °C to +85 °C		1	µA
			T_A = −40 °C to +125 °C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		−0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.7 V ≤ V_{CC} < 2.5 V		−0.5	0.2 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.7 V ≤ V_{CC} < 2.5 V		0.8 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 4. PIN IMPEDANCE CHARACTERISTICS
V_{CC} = 1.7 V to 5.5 V, T_A = –40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Max	Unit
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note 6)	WP Input Current, Address Input Current (A_1, A_2)	$V_{IN} < V_{IH}$, V_{CC} = 5.5 V	75	µA
		$V_{IN} < V_{IH}$, V_{CC} = 3.3 V	50	
		$V_{IN} < V_{IH}$, V_{CC} = 1.7 V	25	
		$V_{IN} > V_{IH}$	2	

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.
6. When not driven, the WP, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull-down is relatively strong; therefore the external driver must be able to supply the pull-down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull-down reverts to a weak current source.

Table 5. A.C. CHARACTERISTICS (Note 7)
V_{CC} = 1.7 V to 5.5 V, T_A = –40 °C to +125 °C, unless otherwise specified.

Symbol	Parameter	Standard V_{CC} = 1.7 V – 5.5 V		Fast V_{CC} = 1.7 V – 5.5 V		Fast–Plus V_{CC} = 2.5 V – 5.5 V T_A = –40 °C to +125 °C		Unit
		Min	Max	Min	Max	Min	Max	
F_{SCL}	Clock Frequency		100		400		1,000	kHz
$t_{HD:STA}$	START Condition Hold Time	4		0.6		0.25		µs
t_{LOW}	Low Period of SCL Clock	4.7		1.3		0.45		µs
t_{HIGH}	High Period of SCL Clock	4		0.6		0.40		µs
$t_{SU:STA}$	START Condition Setup Time	4.7		0.6		0.25		µs
$t_{HD:DAT}$	Data In Hold Time	0		0		0		µs
$t_{SU:DAT}$	Data In Setup Time	250		100		50		ns
t_R (Note 8)	SDA and SCL Rise Time		1,000		300		100	ns
t_F (Note 8)	SDA and SCL Fall Time		300		300		100	ns
$t_{SU:STO}$	STOP Condition Setup Time	4		0.6		0.25		µs
t_{BUF}	Bus Free Time Between STOP and START	4.7		1.3		0.5		µs
t_{AA}	SCL Low to Data Out Valid		3.5		0.9		0.40	µs
t_{DH}	Data Out Hold Time	50		50		50		ns
T_i (Note 8)	Noise Pulse Filtered at SCL and SDA Inputs		50		50		50	ns
$t_{SU:WP}$	WP Setup Time	0		0		0		µs
$t_{HD:WP}$	WP Hold Time	2.5		2.5		1		µs
t_{WR}	Write Cycle Time		5		5		5	ms
t_{PU} (Notes 8, 9)	Power-up to Ready Mode		0.1		0.1		0.1	ms

7. Test conditions according to “A.C. Test Conditions” table.
8. Tested initially and after a design or process change that affects this parameter.
9. t_{PU} is the delay between the time V_{CC} is stable and the device is ready to accept commands.

Table 6. A.C. TEST CONDITIONS

Input Levels	0.2 x V_{CC} to 0.8 x V_{CC}
Input Rise and Fall Times	≤ 50 ns
Input Reference Levels	0.3 x V_{CC}, 0.7 x V_{CC}
Output Reference Levels	0.5 x V_{CC}
Output Load	Current Source: I_L = 3 mA ($V_{CC} \geq$ 2.5 V); I_L = 1 mA (V_{CC} < 2.5 V); C_L = 100 pF

POWER-ON RESET (POR)

The CAT24M01LV incorporates Power-On Reset (POR) circuitry which protects the internal logic against powering up in the wrong state.

The device will power up into Standby mode after V_{CC} exceeds the POR trigger level and will power down into Reset mode when V_{CC} drops below the POR trigger level.

This bi-directional POR behavior protects the device against brown-out failure, following a temporary loss of power.

PIN DESCRIPTION

SCL: The Serial Clock input pin accepts the Serial Clock signal generated by the Master.

SDA: The Serial Data I/O pin receives input data and transmits data stored in EEPROM. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A_1 and A_2: The Address pins accept the device address. These pins have on-chip pull-down resistors.

WP: The Write Protect input pin inhibits all write operations, when pulled HIGH. This pin has an on-chip pull-down resistor.

FUNCTIONAL DESCRIPTION

The CAT24M01LV supports the Inter-Integrated Circuit (I^2C) Bus data transmission protocol, which defines a device that sends data to the bus as a transmitter and a device receiving data as a receiver. Data flow is controlled by a Master device, which generates the serial clock and all START and STOP conditions. The CAT24M01LV acts as a Slave device. Master and Slave alternate as either transmitter or receiver. Up to 4 devices may be connected to the bus as determined by the device address inputs A_1 and A_2.

I^2C Bus Protocol

The I^2C bus consists of two ‘wires’, SCL and SDA. The two wires are connected to the V_{CC} supply via pull-up resistors. Master and Slave devices connect to the 2-wire bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 2).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake-up’ call to all receivers. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP starts the internal Write cycle (when following a Write command) or sends the Slave into standby mode (when following a Read command).

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8-bit serial Slave address. The first 4 bits of the Slave address are set to 1010, for normal Read/Write operations (Figure 3). The next 2 bits, A2, A1, select one of 4 possible memory devices connected on a single I^2C bus. The A2 and A1 bits must match the state of the external address pins. The seventh bit, a16 is the most significant internal address bit. The last bit, $R/\overline{W}$, specifies whether a Read (1) or Write (0) operation is to be performed. To select an internal memory location (data byte) a 17-bit address word is required: a16 bit from the Slave address byte followed by two address bytes.

Acknowledge

After processing the Slave address, the Slave responds with an acknowledge (ACK) by pulling down the SDA line during the 9th clock cycle (Figure 4). The Slave will also acknowledge the byte address and every data byte presented in Write mode. In Read mode the Slave shifts out a data byte, and then releases the SDA line during the 9th clock cycle. If the Master acknowledges the data, then the Slave continues transmitting. The Master terminates the session by not acknowledging the last data byte (NoACK) and by sending a STOP to the Slave. Bus timing is illustrated in Figure 5.

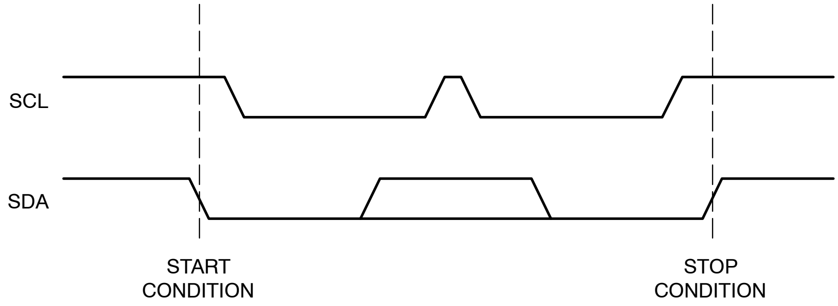


Figure 2. Start/Stop Timing

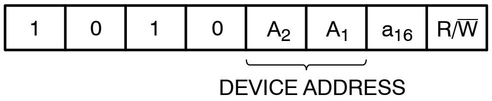


Figure 3. Slave Address Bits

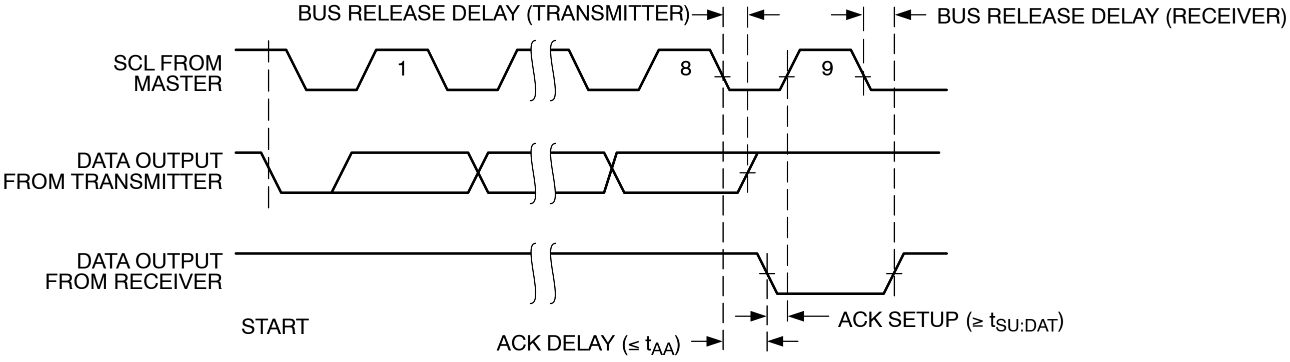


Figure 4. Acknowledge Timing

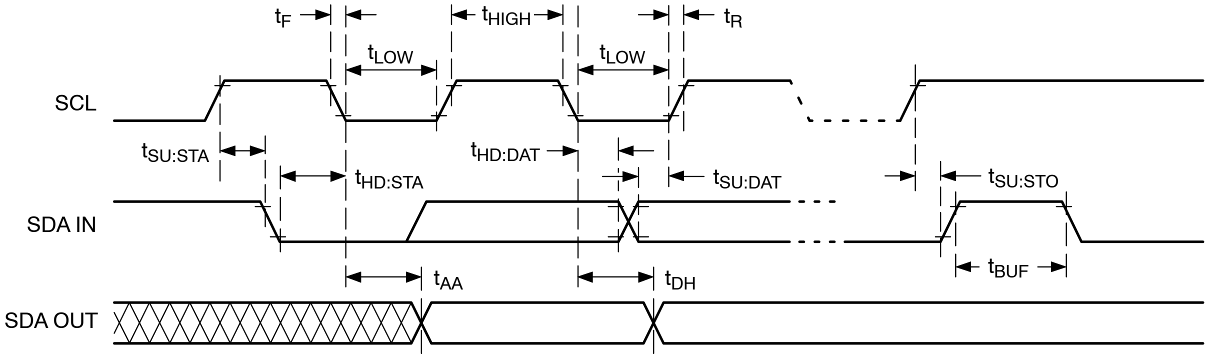


Figure 5. Bus Timing

WRITE OPERATIONS

Byte Write

In Byte Write mode the Master sends a START, followed by Slave address, two byte address and data to be written (Figure 6). The Slave acknowledges all 4 bytes, and the Master then follows up with a STOP, which in turn starts the internal Write operation (Figure 7). During internal Write, the Slave will not acknowledge any Read or Write request from the Master.

Page Write

The CAT24M01LV contains 131,072 bytes of data, arranged in 512 pages of 256 bytes each. The most significant 9 bits of the address word (a16 from the Slave Address byte and most significant Address byte) identify the page and the last 8 bits identify the byte within the page. The 17-bit address word (a16 from the Slave Address byte followed by two address bytes) points to the first byte to be written. Up to 256 bytes can be written in one Write cycle (Figure 8).

The internal byte address counter is automatically incremented after each data byte is loaded. If the Master transmits more than 256 data bytes, then earlier bytes will be overwritten by later bytes in a ‘wrap-around’ fashion (within the selected page). The internal Write cycle starts immediately following the STOP.

Acknowledge Polling

Acknowledge polling can be used to determine if the CAT24M01LV is busy writing or is ready to accept commands. Polling is implemented by interrogating the device with a ‘Selective Read’ command (see READ OPERATIONS).

The CAT24M01LV will not acknowledge the Slave address, as long as internal Write is in progress.

Hardware Write Protection

With the WP pin held HIGH, the entire memory is protected against Write operations. If the WP pin is left floating or is grounded, it has no impact on the operation of the CAT24M01LV. The state of the WP pin is strobed on the last falling edge of SCL immediately preceding the first data byte (Figure 9). If the WP pin is HIGH during the strobe interval, the CAT24M01LV will not acknowledge the data byte and the Write request will be rejected.

Delivery State

The CAT24M01LV is shipped erased, i.e., all bytes are FFh.

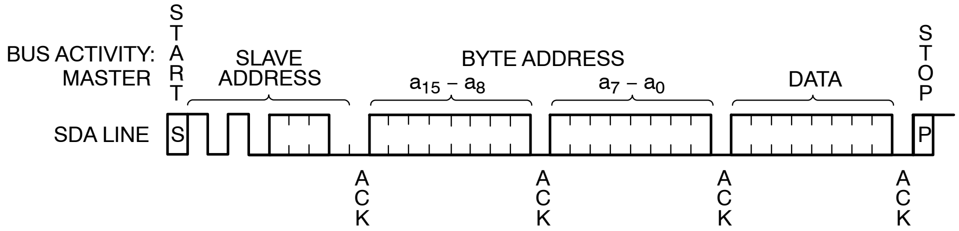


Figure 6. Byte Write Timing

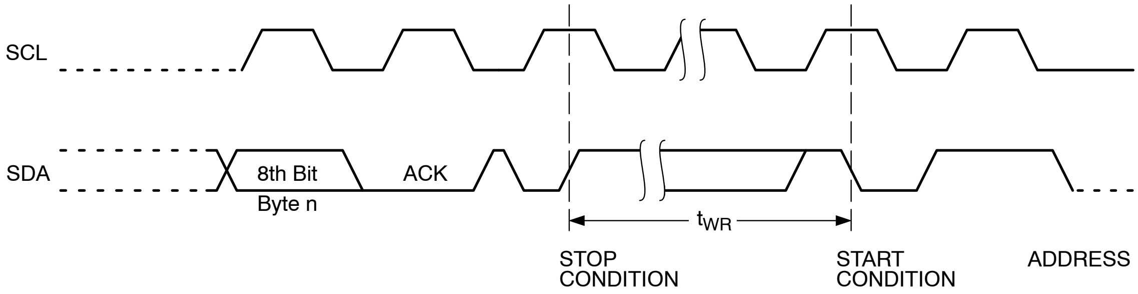


Figure 7. Write Cycle Timing

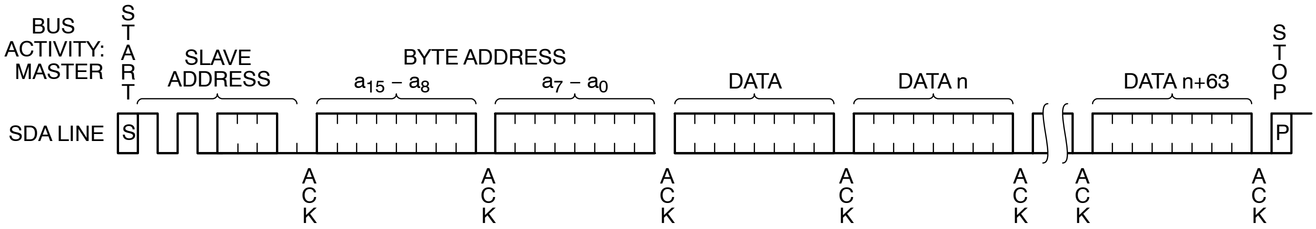


Figure 8. Page Write Timing

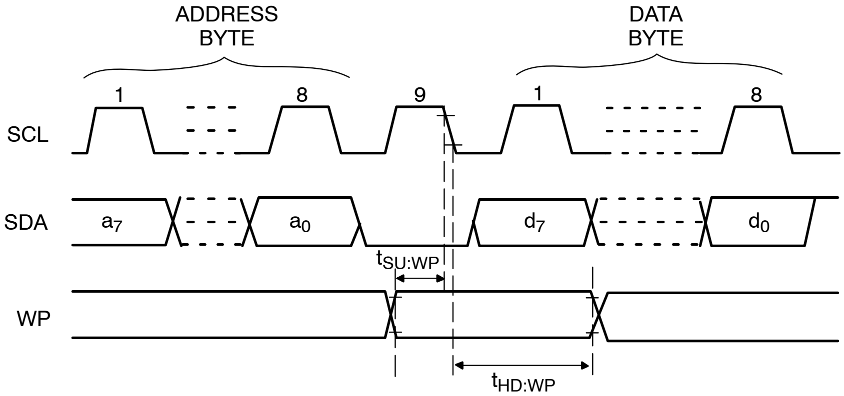


Figure 9. WP Timing

READ OPERATIONS

Immediate Address Read

In standby mode, the CAT24M01LV internal address counter points to the data byte immediately following the last byte accessed by a previous operation. If that ‘previous’ byte was the last byte in memory, then the address counter will point to the 1st memory byte, etc.

When, following a START, the CAT24M01LV is presented with a Slave address containing a ‘1’ in the R/$\overline{\text{W}}$ bit position (Figure 10), it will acknowledge (ACK) in the 9th clock cycle, and will then transmit data being pointed at by the internal address counter. The Master can stop further transmission by issuing a NoACK, followed by a STOP condition.

Selective Read

The Read operation can also be started at an address different from the one stored in the internal address counter. The address counter can be initialized by performing a ‘dummy’ Write operation (Figure 11). Here the START is followed by the Slave address (with the R/$\overline{\text{W}}$ bit set to ‘0’) and the desired two byte address. Instead of following up with data, the Master then issues a 2nd START, followed by the ‘Immediate Address Read’ sequence, as described earlier.

Sequential Read

If the Master acknowledges the 1st data byte transmitted by the CAT24M01LV, then the device will continue transmitting as long as each data byte is acknowledged by the Master (Figure 12). If the end of memory is reached during sequential Read, then the address counter will ‘wrap-around’ to the beginning of memory, etc. Sequential Read works with either ‘Immediate Address Read’ or ‘Selective Read’, the only difference being the starting byte address.

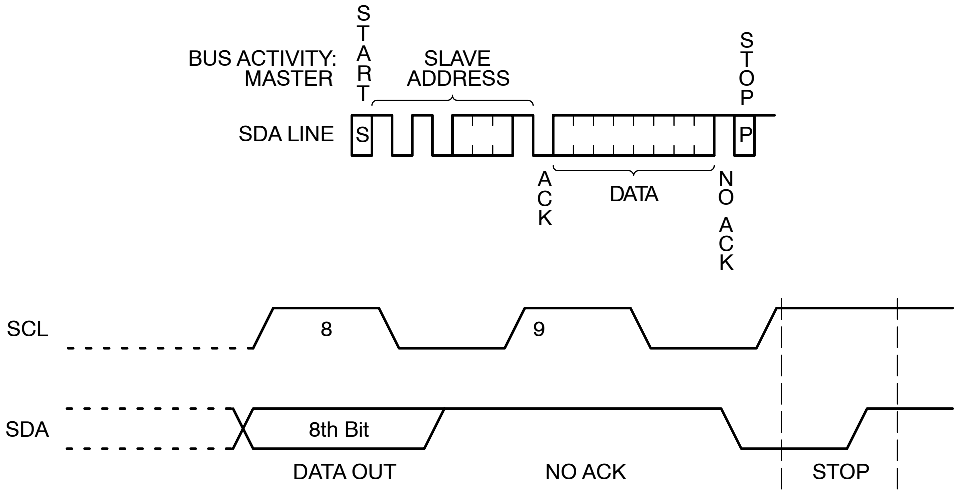


Figure 10. Immediate Address Read Timing

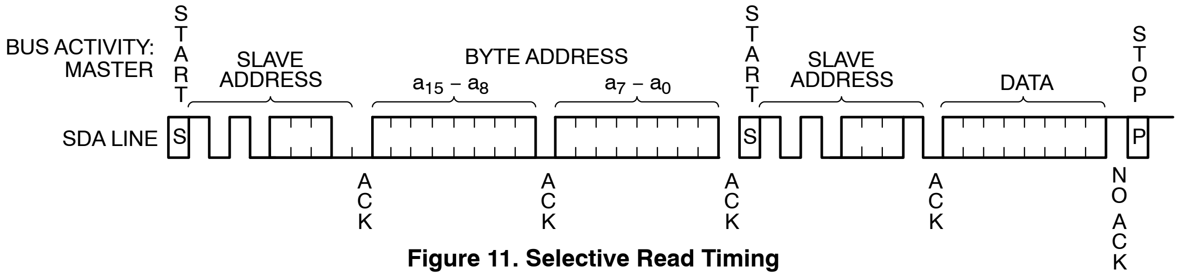


Figure 11. Selective Read Timing

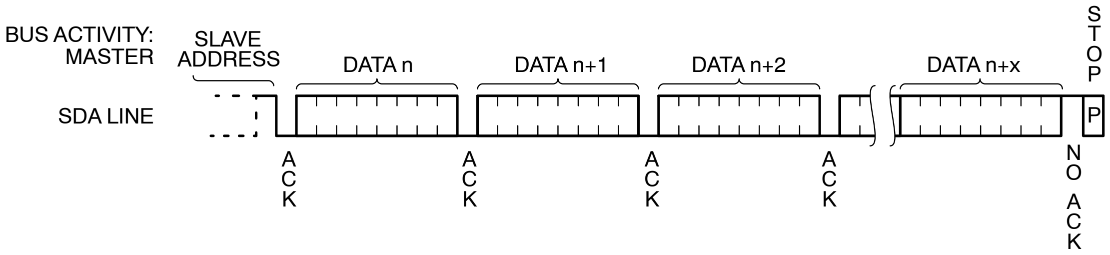


Figure 12. Sequential Read Timing

ORDERING INFORMATION (Note 10)

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24M01DWDLT3G	24M01L	SOIC-8, JEDEC	−40 °C to +125 °C	NiPdAu	3,000 / Tape & Reel
CAT24M01DXDLT2G (In Development)	TBD	SOIC-8, EIAJ	−40 °C to +125 °C	Matte-Tin	2,000 / Tape & Reel
CAT24M01DTDLT3G (In Development)	TBD	TSSOP-8	−40 °C to +125 °C	NiPdAu	3,000 / Tape & Reel
CAT24M01MU8DLT3G (In Development)	TBD	UDFN8	−40 °C to +125 °C	NiPdAu	3,000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

10. All packages are RoHS-compliant (Pb-Free, Halogen-free).

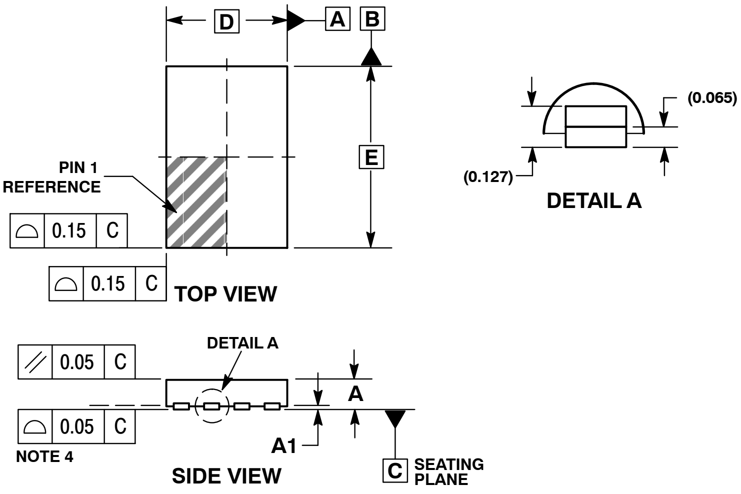
REVISION HISTORY

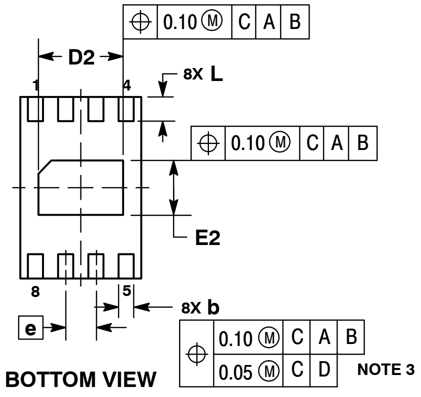
Revision	Description of Changes	Date
2	Rebranded the Data Sheet to **onsemi** format.	08/28/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

PACKAGE DIMENSIONS

UDFN8 3.0x2.0, 0.5P
CASE 517BU
ISSUE O

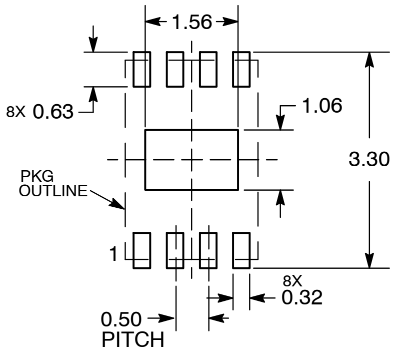




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
b	0.20	0.30
D	2.00 BSC	
D2	1.35	1.45
E	3.00 BSC	
E2	0.85	0.95
e	0.50 BSC	
L	0.35	0.45

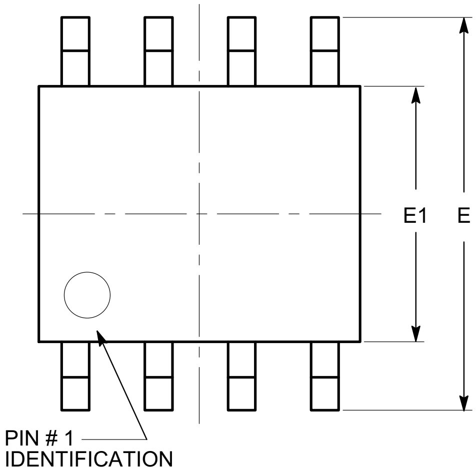
RECOMMENDED MOUNTING FOOTPRINT



DIMENSIONS: MILLIMETERS

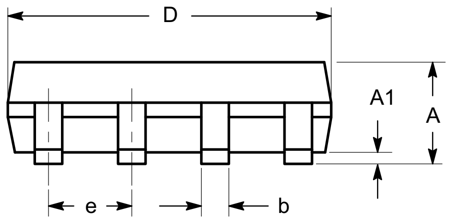
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD
ISSUE O

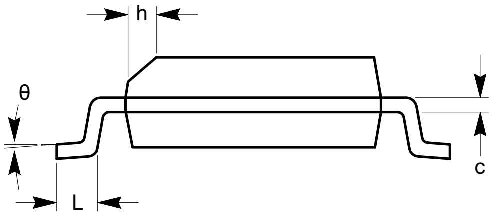


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

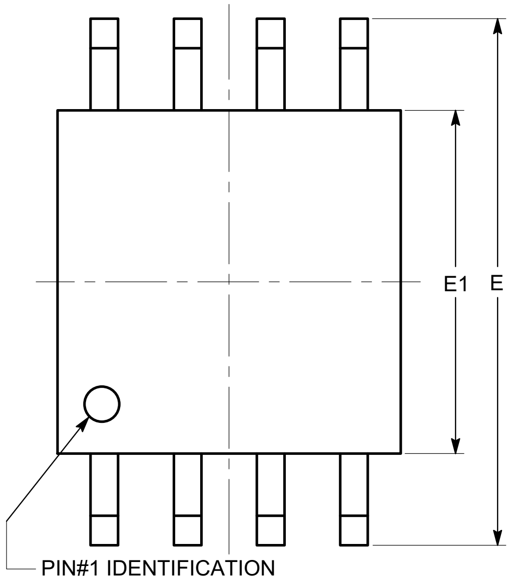


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

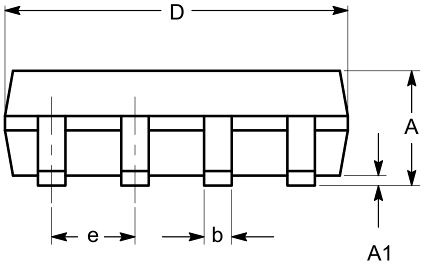
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE
ISSUE O

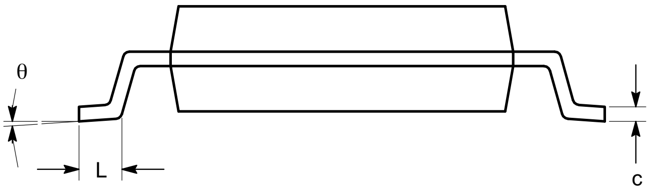


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e	1.27 BSC		
L	0.51		0.76
θ	0º		8º



SIDE VIEW

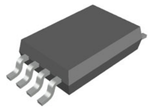


END VIEW

Notes:

(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

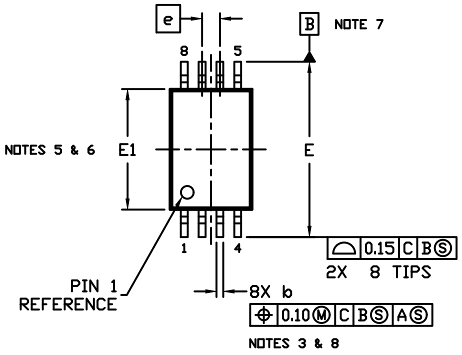
PACKAGE DIMENSIONS



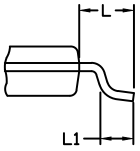
TSSOP8, 4.4x3.0, 0.65P

CASE 948AL
ISSUE A

DATE 20 MAY 2022



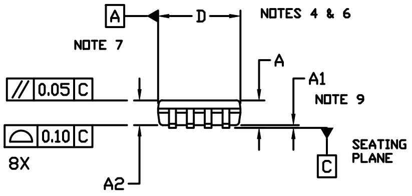
TOP VIEW



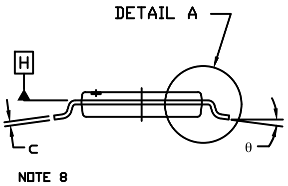
DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5, 2009..
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL NOT BE 0.15 IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM PLANE H.
7. DATUMS A AND B ARE TO BE DETERMINED AT DATUM H.
8. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.25 FROM THE LEAD TIP..
9. A1 IS DEFINED AS THE LOWEST VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY..



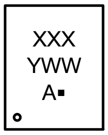
SIDE VIEW



END VIEW

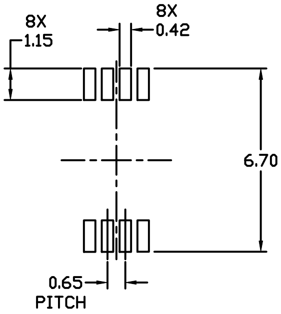
DIM	MILLIMETERS MIN.	MILLIMETERS NOM.	MILLIMETERS MAX.
A	---	---	1.20
A1	0.05	---	0.15
A2	0.80	0.90	1.05
b	0.19	---	0.30
c	0.09	---	0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.70
θ	0°	---	8°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
Y = Year
WW = Work Week
A = Assembly Location
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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